Aurora System

LCFC 联宝科技

LPDDR5(X) Challenge and Simulation

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Outline

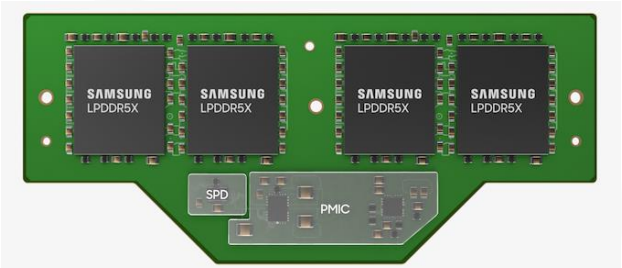
1. LPDDR5(X) Challenges

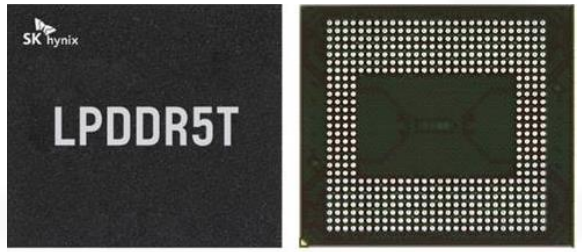
2. Simulation Case and Study

3. AMI Simulation for 8533Mbps Design

LPDDR

DDR SDRAM stands for Double Data Rate SDRAM, which means double data rate SDRAM.
LPDDR is the low-power version of DDR.
From the development of large-scale integrated circuits (IC) and SDRAM to DDR SDRAM, these electronic components have become ubiquitous in everyday life.

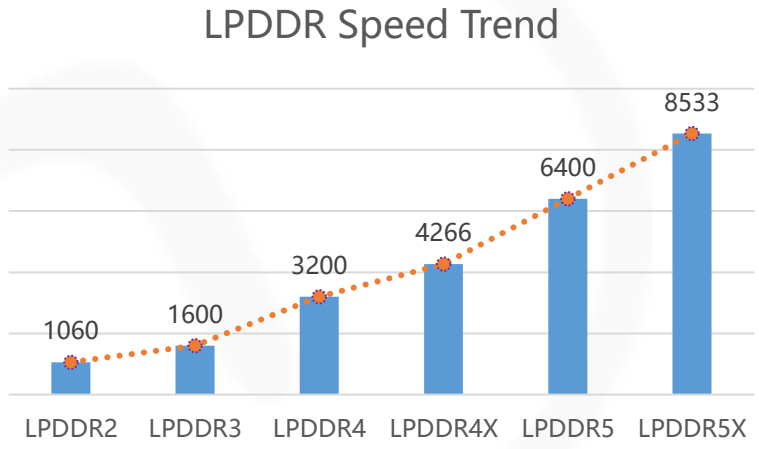




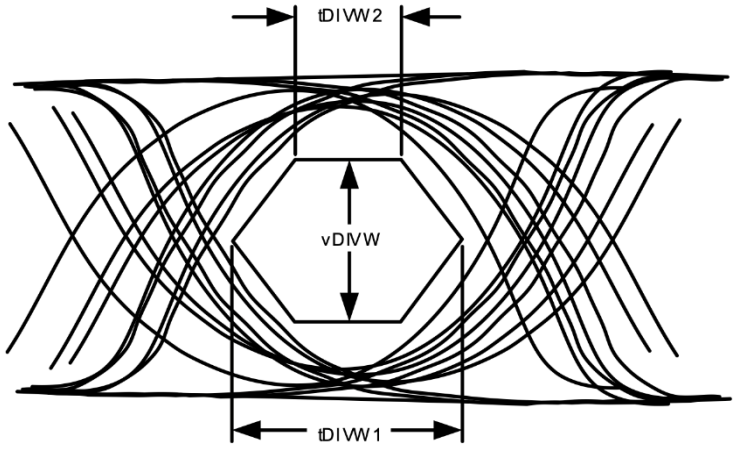
LPDDR Trend

1. It has continuously evolved toward higher data rates, wider bandwidth, and improved energy efficiency.
2. Currently, it has advanced to LPDDR5X with speeds of up to 8.533 Gbps, and even LPDDR5T reaching 9.6 Gbps.
3. The interface voltage has also dropped from the initial 1.2V to 0.5V.

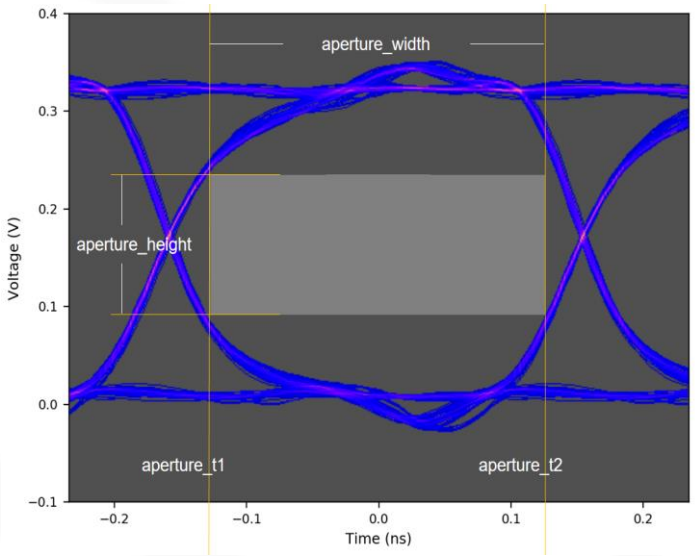
LPDDR Generations					
	LPDDR3	LPDDR4	LPDDR4X	LPDDR5	LPDDR5X
Spec Release Time	2012	2014	2016	2019	2022
Max Density	32Gbit	64Gbit		32Gbit	
Max Data Rate	2133Mbps	3200Mbps	4266Mbps	6400Mbps	8533Mbps
Channel	1	2		1	
Width	32-bits	32-bits(2x16-bit)		16-bits	
Vdd	1.2V	1.1V		1.05V	
Vddq	1.2V	1.1V	0.6V	0.5V	



LPDDR5(X) Eye Mask and Eye Aperture



Hexagonal eye-mask, LPDDR5 JEDEC standard



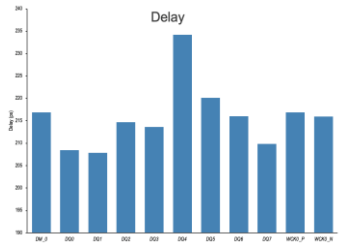
	3733Mbps~6400Mbps	7500Mbps~8533Mbps
tDIVW1	0.35 * UI	
tDIVW2	0.18 * UI	
vDIVW	100mV	80mV

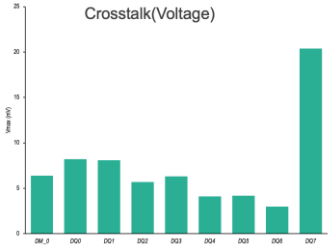
	3733Mbps~6400Mbps	7500Mbps~8533Mbps
Aperture_Height	100mV	80mV
Aperture_Width	0.35 * UI {Depends on LPDDR5(X) IP}	

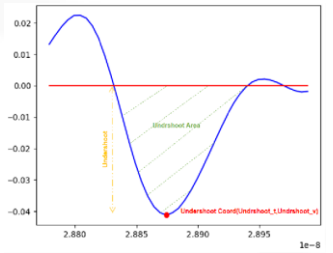
DDR SI Simulation Pain Points

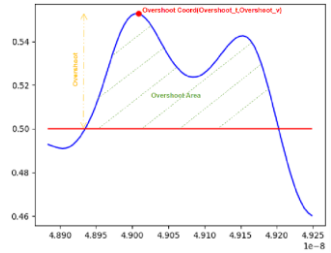
The higher speed and lower interface voltage present greater design challenges for the timing and voltage margins of LPDDR.

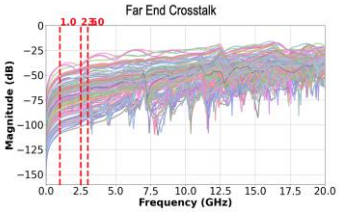
1. Dual-channel, Dual Rank, and multiple IC corner cause large simulation scale.
2. A wide variety of signal lines, such as DQ, RDQS, WCK, CA, CS and CLK.
3. Too many metrics in simulation results:
    1). eye diagram, eye width, eye height, eye aperture;
    2). IL, RL, NEXT, FEXT Crosstalk, delay and skew

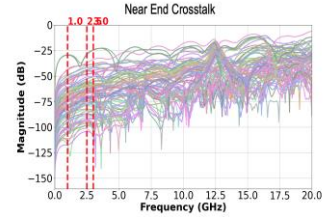


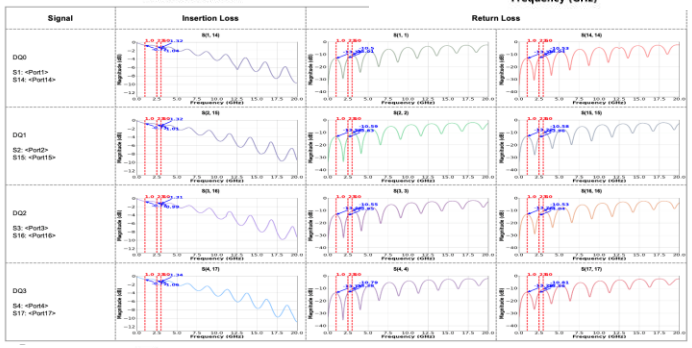


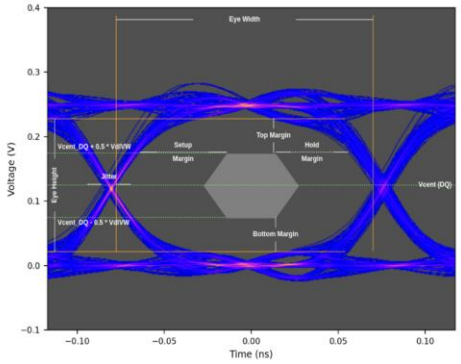




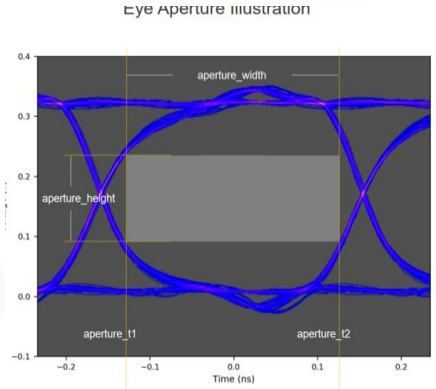






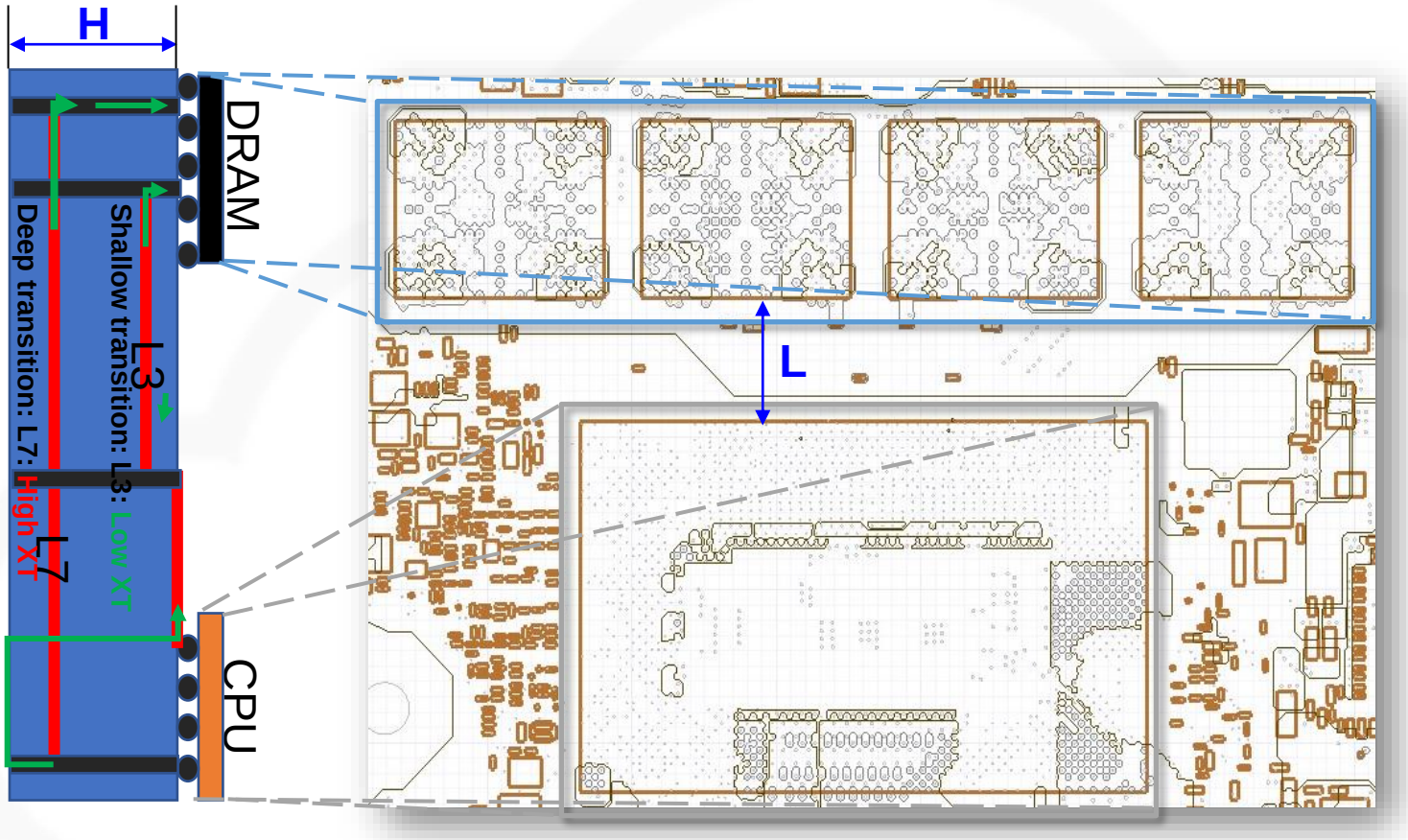


Eye Width (ps)	146.0
Eye Height (mV)	186.4
Jitter (ps)	10.2
Top Margin (mV)	42.0
Bottom Margin (mV)	44.7
Setup Margin (ps)	44.8
Hold Margin (ps)	44.9



	DQ0	DQ1	DQ2	DQ3
aperture_height (V)	0.1	0.1	0.1	0.1
aperture_t1 (ps)	-51.2257	-61.0498	-48.8866	-53.0969
aperture_t2 (ps)	59.6463	54.0326	58.2429	40.9338
aperture_width (ps)	110.872	115.0823	107.1295	94.0307
width spec (ps)	100	100	100	100
Pass / Fail	pass	pass	pass	fail

LPDDR5(X) Layout Design challenge



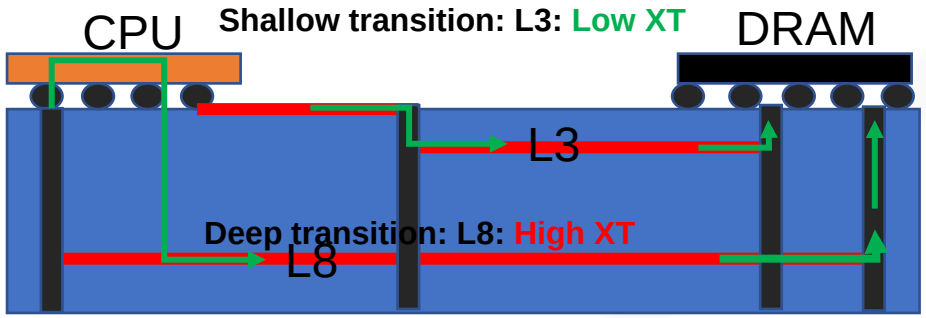
LPDDR5(X) Layout Design challenge

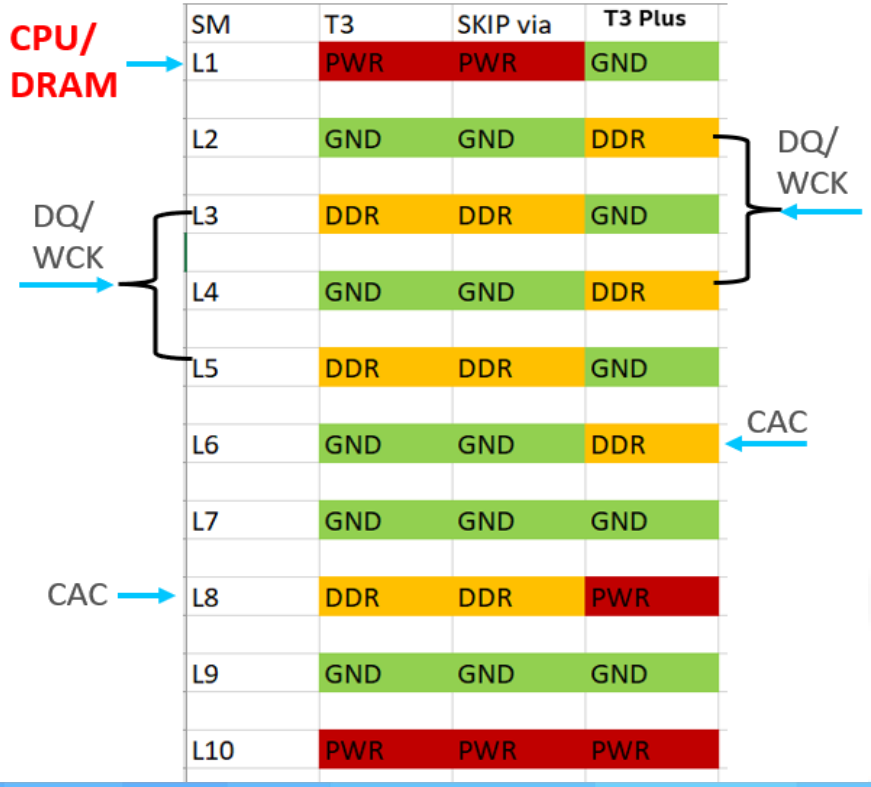
Trace XTL	Via XTL	Via Stub
Trace width(W)、Trace Space(S)、The distance between the routing layer and the reference layer (h)	Via space(S') 、Signal routing layer distribution (Layer)、Via size(D)	Signal routing layer distribution (Layer)、PCB Thickness (H)、Cost(C)
CPU-Memory spacing L is limited by system design S ↓	Limited by system design and planning **Layers** are limited	Limited by system design and planning **Layers** are limited
PCB Stack up Material DK Influence W ↑	CPU-Memory spacing L is limited by system design S' ↓	The total thickness of the PCB is limited by the whole system. Via Stub ↑
The total thickness of the PCB is limited by the whole system. h ↓	Limited by PCB processing technology D ↑	Back drilling is limited by design cost (C) Via Stub ↑

What's more?

System size constraints, cost control, PCB manufacturing process limitations, and copper thickness restrictions due to power stability requirements…..

Study Background





SM	T3	SKIP via	T3 Plus
L1	PWR	PWR	GND
L2	GND	GND	DDR
L3	DDR	DDR	GND
L4	GND	GND	DDR
L5	DDR	DDR	GND
L6	GND	GND	DDR
L7	GND	GND	GND
L8	DDR	DDR	PWR
L9	GND	GND	GND
L10	PWR	PWR	PWR

Platform design Recommendation

- Layer assignment: DQ on shallow transitions & CAC on deeper transitions.
- PCB Thickness: recommends PCB thickness less than 0.9mm to avoid long stubs for DQ signals.
- PCB Type: recommends PCB to achieve data rate 7500Mbps

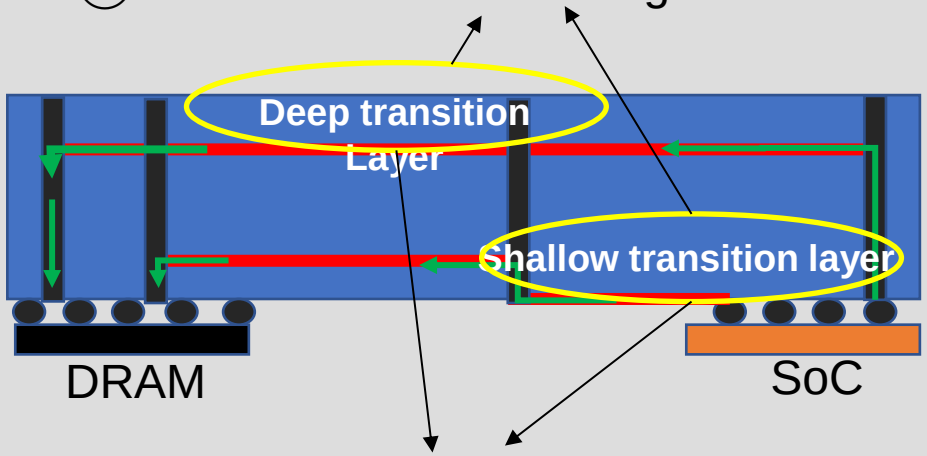
Study Topic?

1. Better solution for Memory Layer assignment?
2. PCB thickness 1.0mm is feasibility?
3. Our PCB type can achieve the data rate 7500Mbps?

Simulation scheme description

Simulation condition

①the different layer
②the different electrical length thu via
③the different via stub length



①the same routing
②the same trace width/space
③the same distance to reference layer

Key Result

Crosstalk in ratio
Insertion loss
Eye diagram/ Aperture

① Check the eye diagram with JEDEC LPDDR5 eye mask
② DQ signal speed=**7500Mbps**

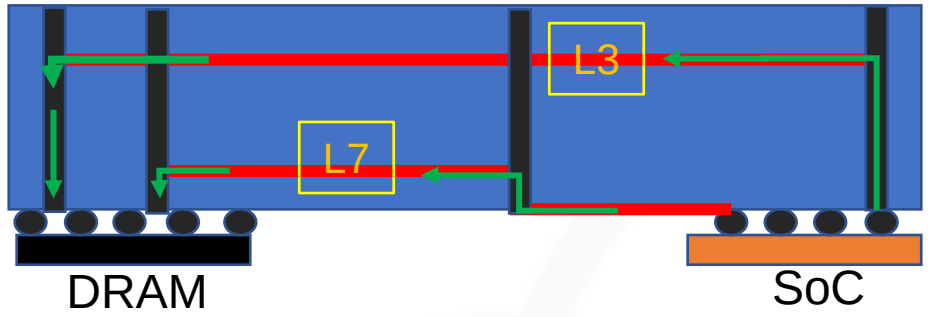
Color	Name	Type	Thickness (mm)	Material	Conductivity (S/m)	Dielectric Fill	Dielectric constant
	UNNAMED_000	DIELECTRIC	0	AIR	0		1
	UNNAMED_001	DIELECTRIC	0.013	SOLDERMASK	0		4
	TOP	METAL	0.03	COPPER	5.959E+07	TOP_FILL	3.7
	UNNAMED_003	DIELECTRIC	0.07	FR-4	0		3.4
	L2GND	METAL	0.015	COPPER	5.959E+07	L2GND_FILL	3.55
	UNNAMED_005	DIELECTRIC	0.075	FR-4_1	0		3.7
	L3	METAL	0.015	COPPER	5.959E+07	FR-4_1	3.7
	L4GND	METAL	0.03	COPPER	5.959E+07	FR-4_1	3.7
	L5VCC	METAL	0.03	COPPER	5.959E+07	FR-4_1	3.7
	UNNAMED_011	DIELECTRIC	0.08	FR-4_1	0		3.7
	L6	METAL	0.03	COPPER	5.959E+07	FR-4_1	3.7
	UNNAMED_013	DIELECTRIC	0.1	FR-4_1	0		3.7
	L7GND_VAL	METAL	0.03	COPPER	5.959E+07	FR-4_1	3.7
	UNNAMED_015	DIELECTRIC	0.06	FR-4_1	0		3.7
	L8_VAL	METAL	0.03	COPPER	5.959E+07	FR-4_1	3.7
	UNNAMED_017	DIELECTRIC	0.05	FR-4_1	0		3.7
	L9_PWR_VAL	METAL	0.03	COPPER	5.959E+07	FR-4_1	3.7
	UNNAMED_019	DIELECTRIC	0.06	FR-4_1	0		3.7
	L10_VAL	METAL	0.03	COPPER	5.959E+07	FR-4_1	3.7
	UNNAMED_021	DIELECTRIC	0.1	FR-4_1	0		3.7
	L11VCC	METAL	0.03	COPPER	5.959E+07	FR-4_1	3.7
	UNNAMED_023	DIELECTRIC	0.08	FR-4_1	0		3.7
	L12	METAL	0.03	COPPER	5.959E+07	FR-4_1	3.7
	UNNAMED_025	DIELECTRIC	0.1	FR-4_1	0		3.7
	L13GND	METAL	0.03	COPPER	5.959E+07	FR-4_1	3.7
	UNNAMED_027	DIELECTRIC	0.1	FR-4_1	0		3.7
	L14	METAL	0.015	COPPER	5.959E+07	FR-4_1	3.7
	UNNAMED_029	DIELECTRIC	0.075	FR-4_1	0		3.7
	L15GND	METAL	0.015	COPPER	5.959E+07	L15GND_FILL	3.55
	UNNAMED_031	DIELECTRIC	0.07	FR-4	0		3.4
	BOTTOM	METAL	0.03	COPPER	5.959E+07	BOTTOM_FILL	3.7
	UNNAMED_033	DIELECTRIC	0.013	SOLDERMASK	0		4
	UNNAMED_034	DIELECTRIC	0	AIR	0		1

Via length=13.19mil

Worst layer

Overview---T3+ PCB

- Simulation Settings



Key factor identify:

- Via Crosstalk
- Via stub
- PCB Thickness

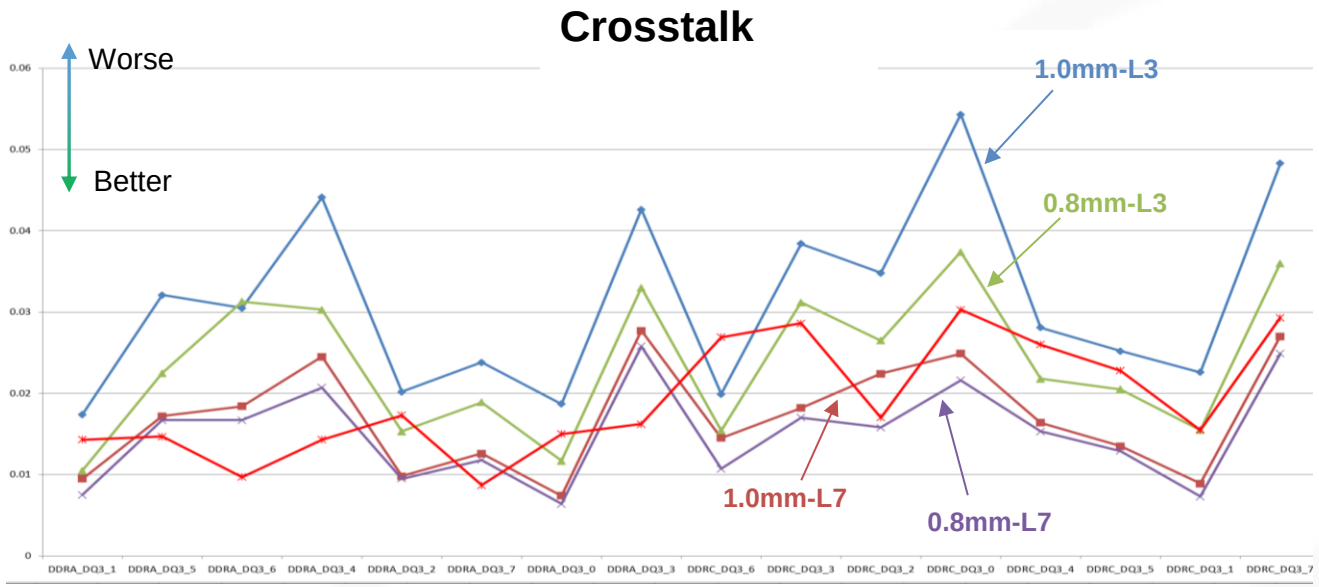
Layer No.	Layer Name	Material Type	Material	Thickness Unit:mil	Dk(3.4~4) @1Ghz	Df(0.007~0.009) @1Ghz
		SolderMask	SolderMask	0.8	4	
1	TOP	Copper+Plating	1/3oz+Plating	1.4		
		pp	1067 RC69%	1.875	3.29	0.0090
2	GND	Copper	1OZ	1.3		
		CORE	2.5-1/H(1078)	2.5	3.81	0.0080
3	IN1	Copper	1/2OZ	0.65		
		pp	1067MR RC71%	2.075	3.24	0.0090
4	VCC	Copper	1/2OZ	0.65		
		CORE	2.5-H/H(1078)	2.5	3.81	0.0080
5	IN2	Copper	1OZ	1.3		
		pp	2116MR*2 RC53%	8.75	3.70	0.0080
6	IN3	Copper	1OZ	1.3		
		CORE	2.5-H/H(1078)	2.5	3.81	0.0080
7	GND	Copper	1/2OZ	0.65		
		PP	1067MR RC71%	2.075	3.24	0.0090
8	IN4	Copper	1/2OZ	0.65		
		CORE	2.5-1/H(1078)	2.5	3.81	0.0080
9	GND3	Copper	1OZ	1.3		
		PP	1067 RC69%	1.875	3.29	0.0090
10	BOTTOM	Copper+Plating	1/3oz+Plating	1.4		
		SolderMask	SolderMask	0.8	4	

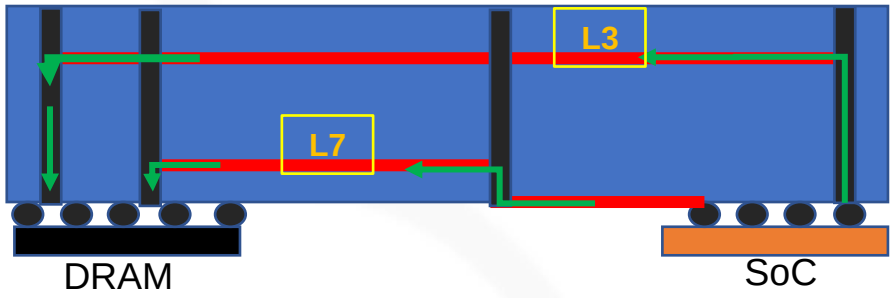
7.08mil
29.53mil
26.8mil
9.8mil
L3
L7

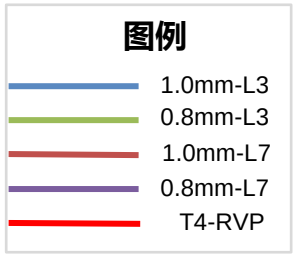
Layer No.	Layer Name	Material Type	Material	Thickness Unit:mil	Dk(3.4~4) @1Ghz	Df(0.007~0.009) @1Ghz
		SolderMask	SolderMask	0.8	4	
1	TOP	Copper+Plating	1/3oz+Plating HTE	1.4		
		pp	1067 RC69%	1.875	3.19	0.0090
2	GND	Copper	1OZ HTE	1.3		
		CORE	2.5-H/H(1078)	2.5	3.81	0.0080
3	IN1	Copper	1/2OZ HTE	0.65		
		pp	1067MR RC71%	2.075	3.19	0.0090
4	VCC	Copper	1/2OZ HTE	0.65		
		CORE	2.5-H/H(1078)	2.5	3.81	0.0080
5	IN2	Copper	1/2OZ HTE	0.65		
		pp	1067HR RC73%	2.275	3.19	0.0090
6	IN3	Copper	1/2OZ HTE	0.65		
		CORE	2.5-H/H(1078)	2.5	3.81	0.0080
7	GND	Copper	1/2OZ HTE	0.65		
		PP	1067MR RC71%	2.075	3.19	0.0090
8	IN4	Copper	1/2OZ HTE	0.65		
		CORE	2.5-H/H(1078)	2.5	3.81	0.0080
9	GND3	Copper	1OZ HTE	1.3		
		PP	1067 RC69%	1.875	3.19	0.0090
10	BOTTOM	Copper+Plating	1/3oz+Plating HTE	1.4		
		SolderMask	SolderMask	0.8	4	

7.08mil
21.75mil
19.03mil
9.8mil
L3
L7

DQ crosstalk Simulation Result



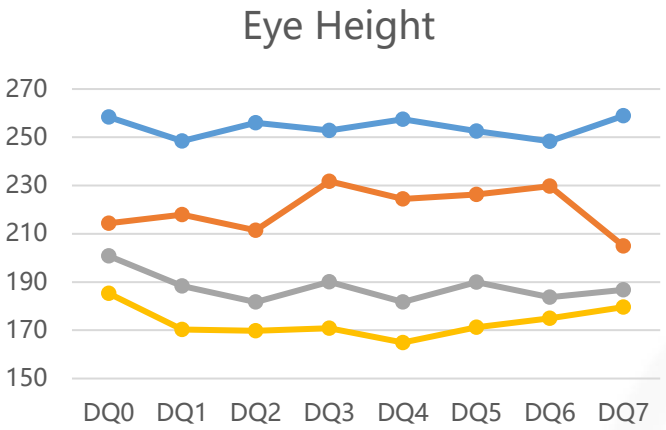


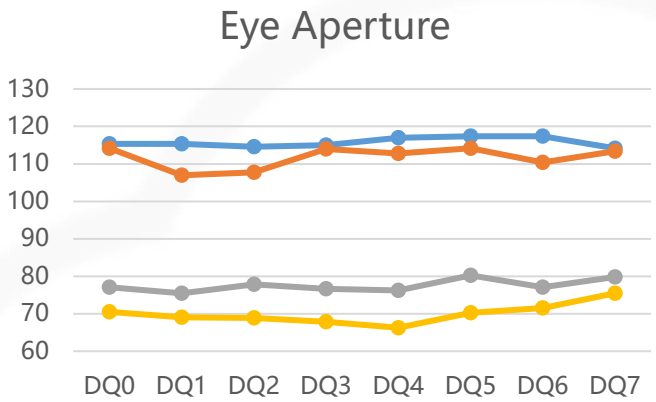


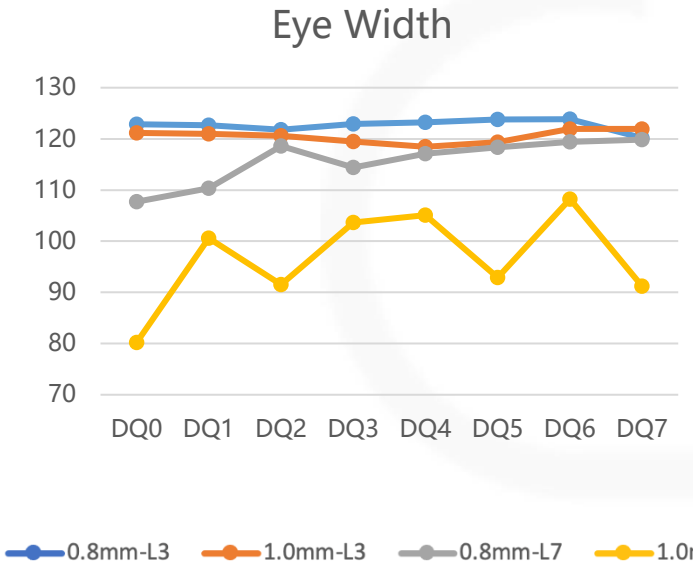
Conclusion:

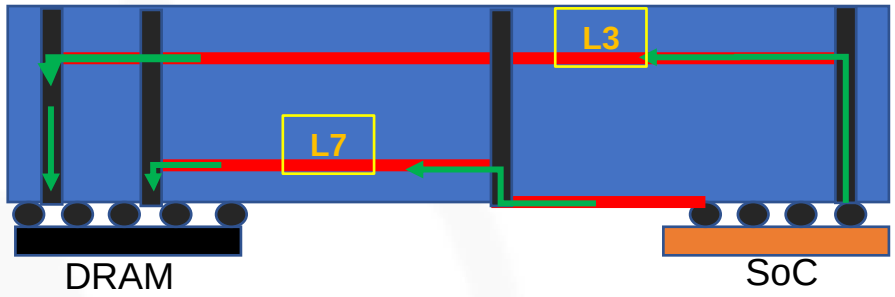
Via coupling length affects via crosstalk. The farther the layer is changed (L3), the worse the crosstalk is.

Eye Mask & Eye Aperture Simulation Result









Conclusion:

Via stub affects Eye Height and Eye Aperture. The closer the layer change (L7), the worse the eye height. Comprehensive evaluation: Based on the eye diagram results, it is recommended that DQ go to the layer far from the layer change.

Single Rank vs Dual Rank

<table>
<tr><th>Memory Die pkg Type</th><th>Topology</th><th>Simulation result DQ</th><th>Simulation result CA</th></tr>
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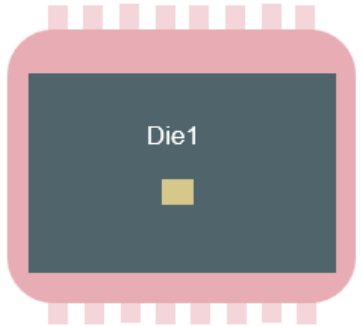
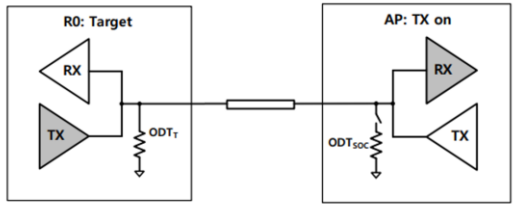
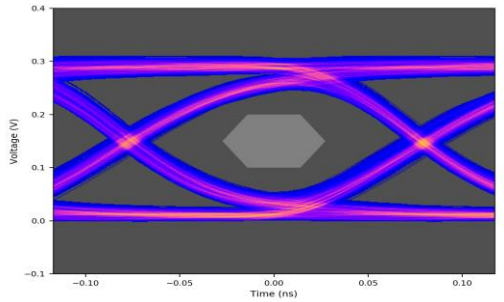
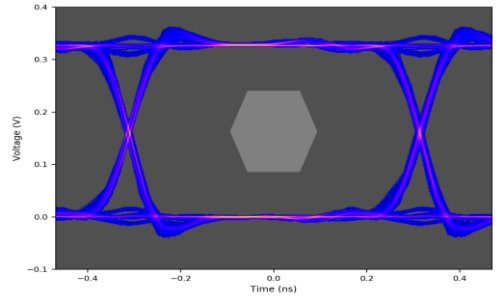
<td> 

Single Rank</td>
<td> 

[Write case]</td>
<td> 

<table>
<tr><td>Eye Width (ps)</td><td>127.1</td></tr>
<tr><td>Eye Height (mv)</td><td>168.6</td></tr>
<tr><td>Jitter (ps)</td><td>27.0</td></tr>
</table></td>
<td> 

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<tr><td>Eye Width (ps)</td><td>606.5</td></tr>
<tr><td>Eye Height (mv)</td><td>317.9</td></tr>
<tr><td>Jitter (ps)</td><td>16.8</td></tr>
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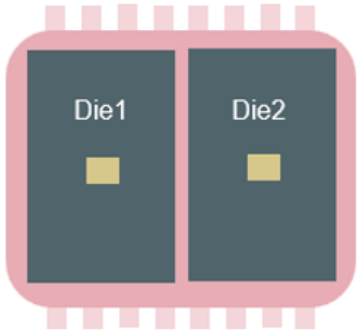
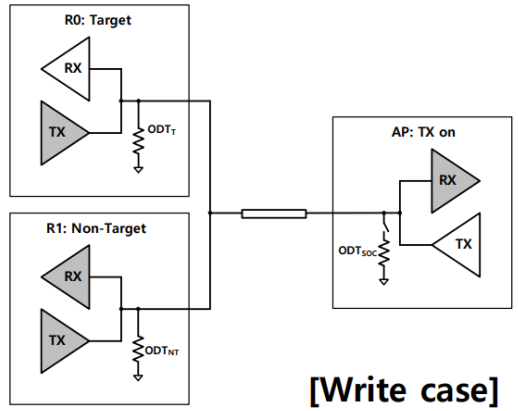
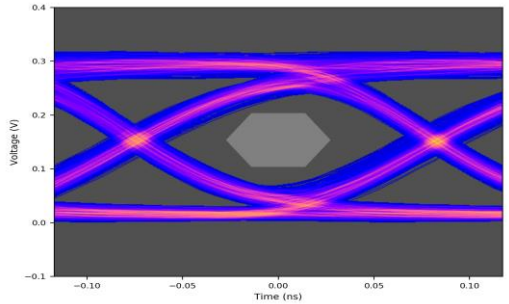
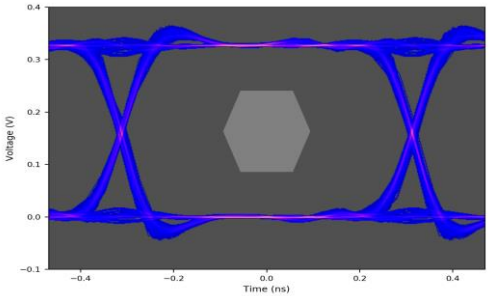
<td> 

Dual Rank</td>
<td> 

[Write case]</td>
<td> 

<table>
<tr><td>Eye Width (ps)</td><td>116.6</td></tr>
<tr><td>Eye Height (mv)</td><td>137.6</td></tr>
<tr><td>Jitter (ps)</td><td>35.9</td></tr>
</table></td>
<td> 

<table>
<tr><td>Eye Width (ps)</td><td>599.0</td></tr>
<tr><td>Eye Height (mv)</td><td>316.6</td></tr>
<tr><td>Jitter (ps)</td><td>25.3</td></tr>
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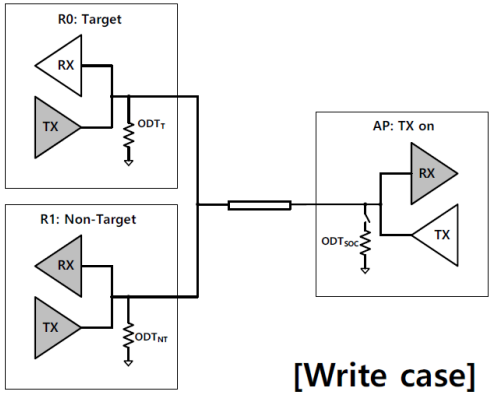
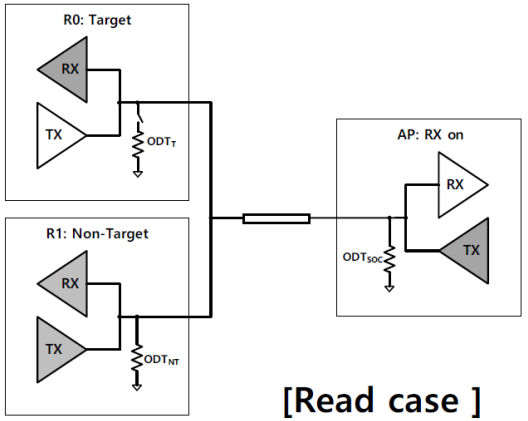
</table>

Normal mode vs Non-Target ODT



[Write case]



[Read case]

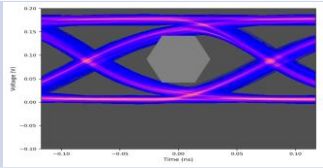
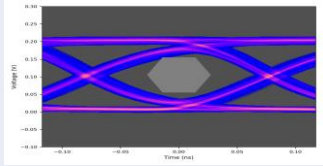
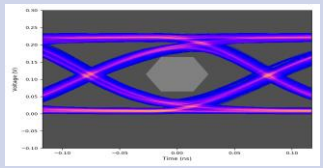
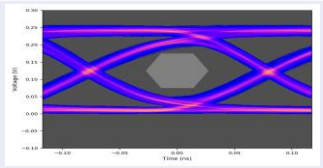
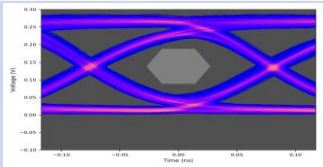
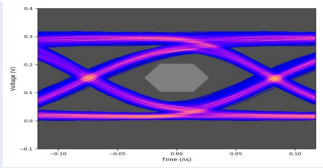
Table 280 — Normal Mode vs. NT-ODT Mode for Write Operation

Mode MR11 OP[3]	Target Rank ODT	Non-Target Rank ODT	Equivalent ODT of 2-Rank DRAM
OP[3]=0 (Normal Mode)	MR11 OP[2:0] (ODT_T)	Disable	ODT_T
OP[3]=1 (NT-ODT Mode)	MR11 OP[2:0] (ODT_T)	MR41 OP[7:5] (ODT_{NT})	ODT_T || ODT_{NT}
OP[3]=1 (NT-ODT Mode)	Disable	MR41 OP[7:5] (ODT_{NT})	ODT_{NT}

Table 281 — Normal Mode vs. NT-ODT Mode for Read Operation

Mode MR11 OP[3]	Non-Target Rank ODT	SoC Rx ODT	Equivalent ODT for RD operation	MR17 OP[2:0] (SoC ODT for DRAM Pull-Up Cal.)
OP[3]=0 (Normal Mode)	Disable	ODT_{SOC}	ODT_{SOC}	ODT_{SOC}
OP[3]=1 (NT-ODT Mode)	MR41 OP[7:5] (ODT_{NT})	ODT_{SOC}	ODT_{NT} || ODT_{SOC}	ODT_{NT} || ODT_{SOC}[1]
NOTE 1 Since SoC ODT of MR17 can only support RZQ/n (n=1,2,3,4,5,6), (ODTNT||ODTSOC) should be one of RZQ/1, RZQ/2, RZQ/3, RZQ/4, RZQ/5, and RZQ/6.				

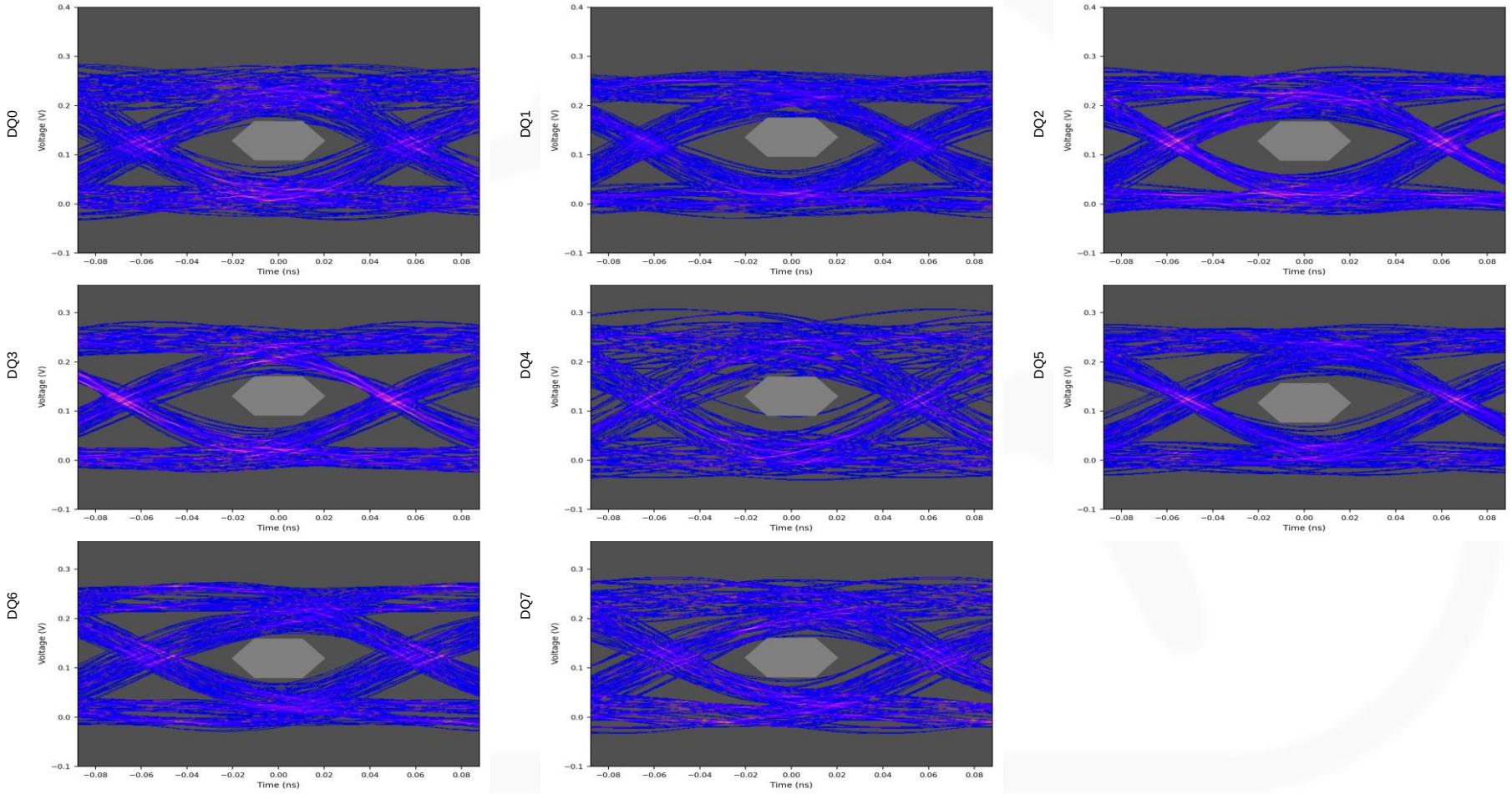
Non-Target VS ODTs Simulation Results

PU (ohm)	Target ODT(ohm)	Non-Target ODT(ohm)	Eye Diagram		
40	60	40		Eye Width (ps)	117.1
				Eye Height (mv)	83.5
				Jitter (ps)	37.2
		60		Eye Width (ps)	122.1
				Eye Height (mv)	104.6
				Jitter (ps)	31.2
		80		Eye Width (ps)	124.5
				Eye Height (mv)	114.6
				Jitter (ps)	28.4
		120		Eye Width (ps)	125.9
				Eye Height (mv)	126.0
				Jitter (ps)	29.4
		240		Eye Width (ps)	125.8
				Eye Height (mv)	136.0
				Jitter (ps)	29.1
		Disable (open)		Eye Width (ps)	116.6
				Eye Height (mv)	137.6
				Jitter (ps)	35.9

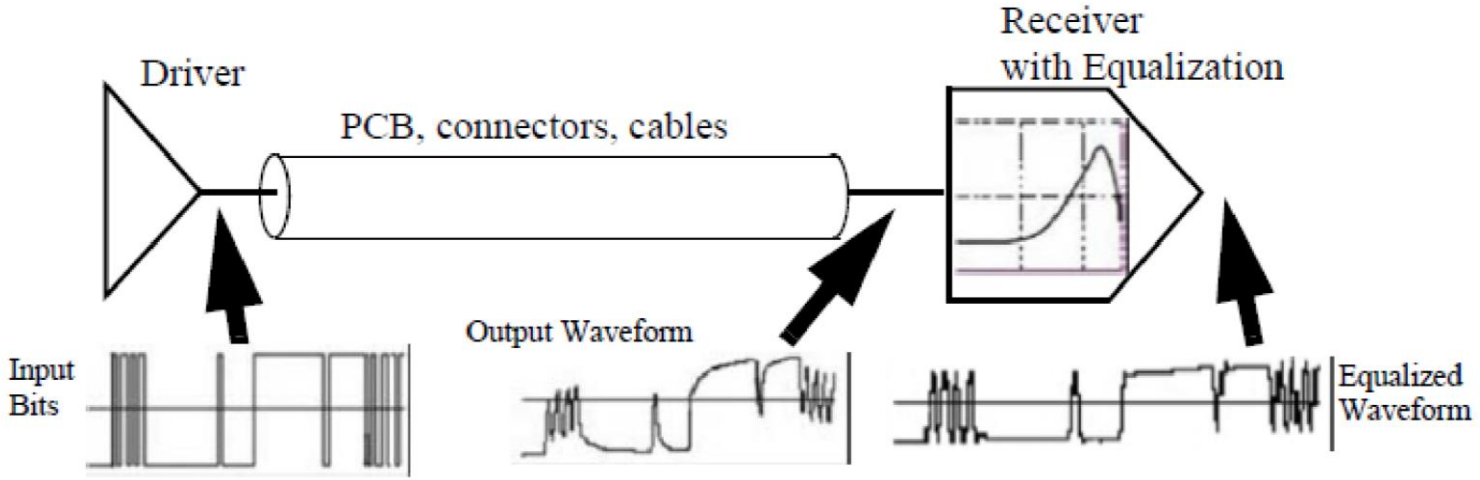
Conclusion:

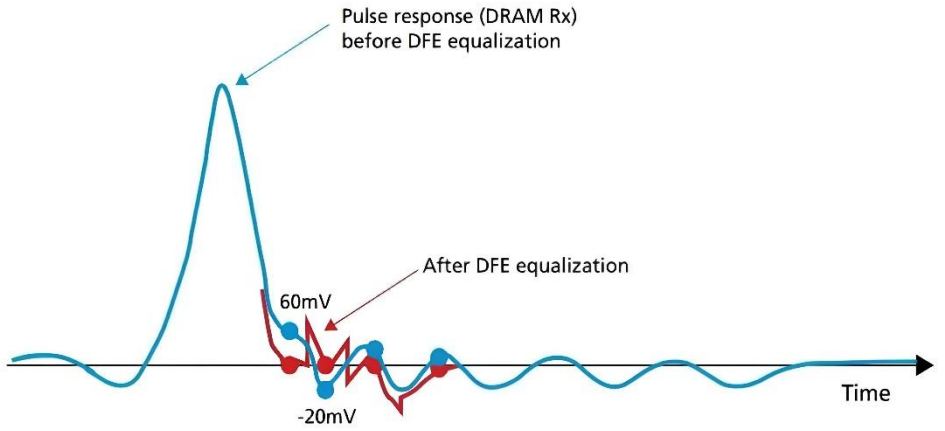
The matching of Non-Target ODT will affect the signal quality. Taking the write direction as an example, the equivalent ODT = ODTT//ODTNT; therefore: the larger the ODTNT, the larger the equivalent ODT, the higher the end voltage divider, and the larger the simulation result of the eye height; at the same time, the equivalent ODT also needs to consider the impedance continuity. The closer the parallel impedance is to the characteristic impedance of the channel and pkg, the smaller the reflection and the larger the eye width.

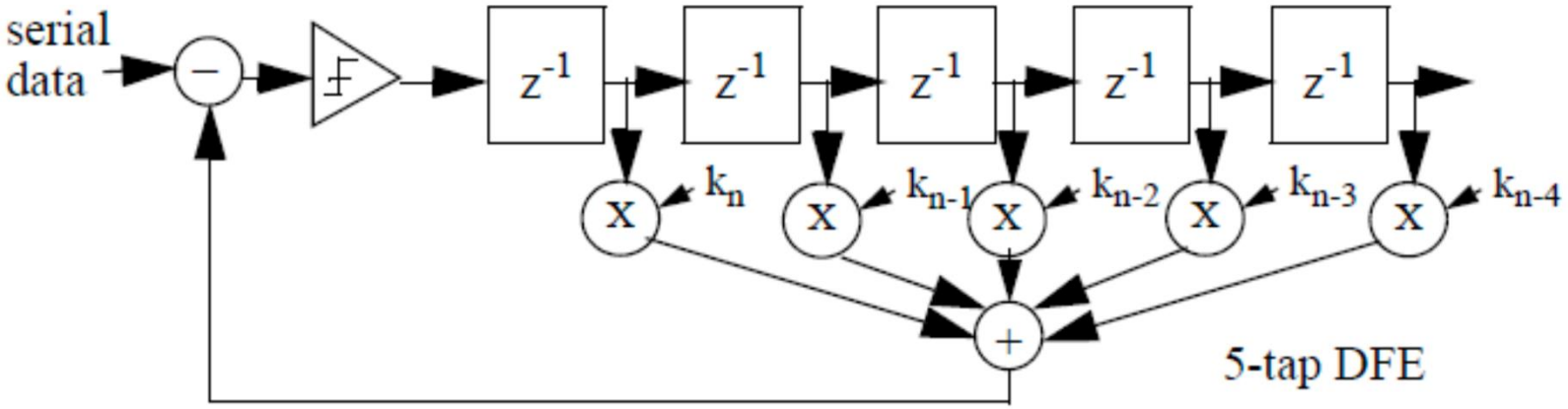
How about 8533Mbps?



DFE(Decision Feedback Equalization)

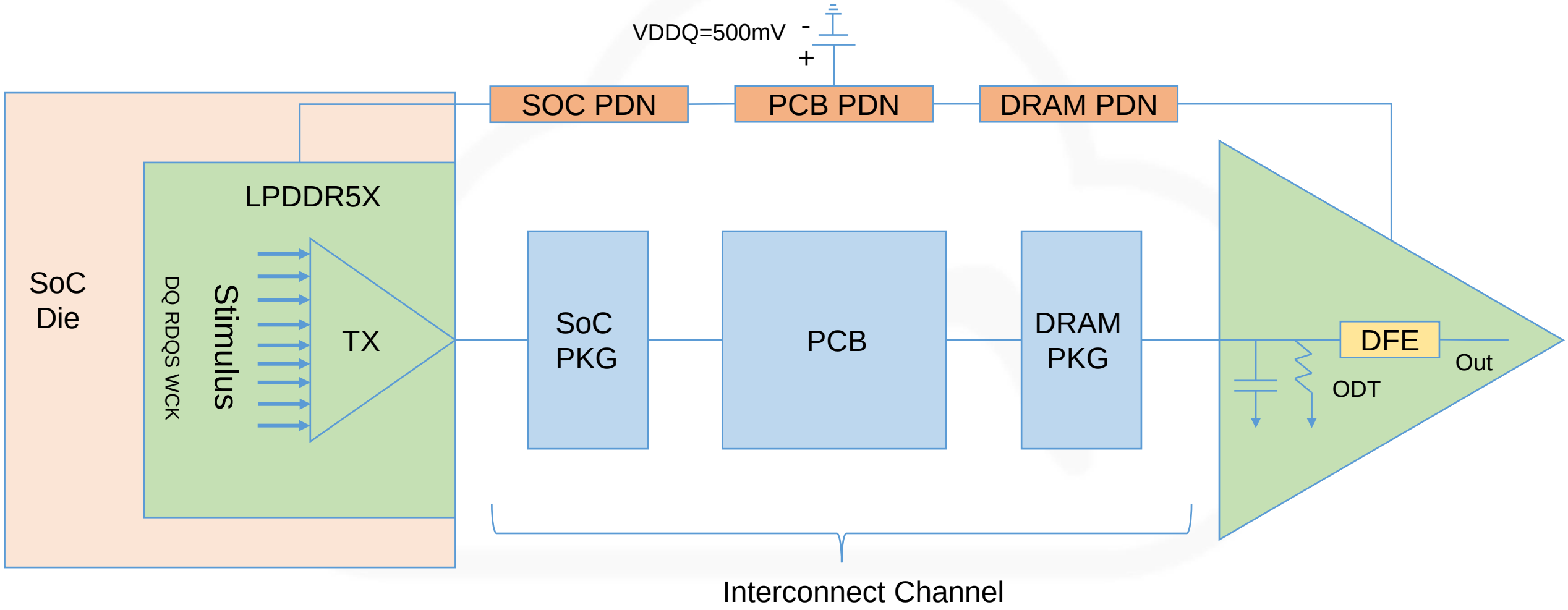




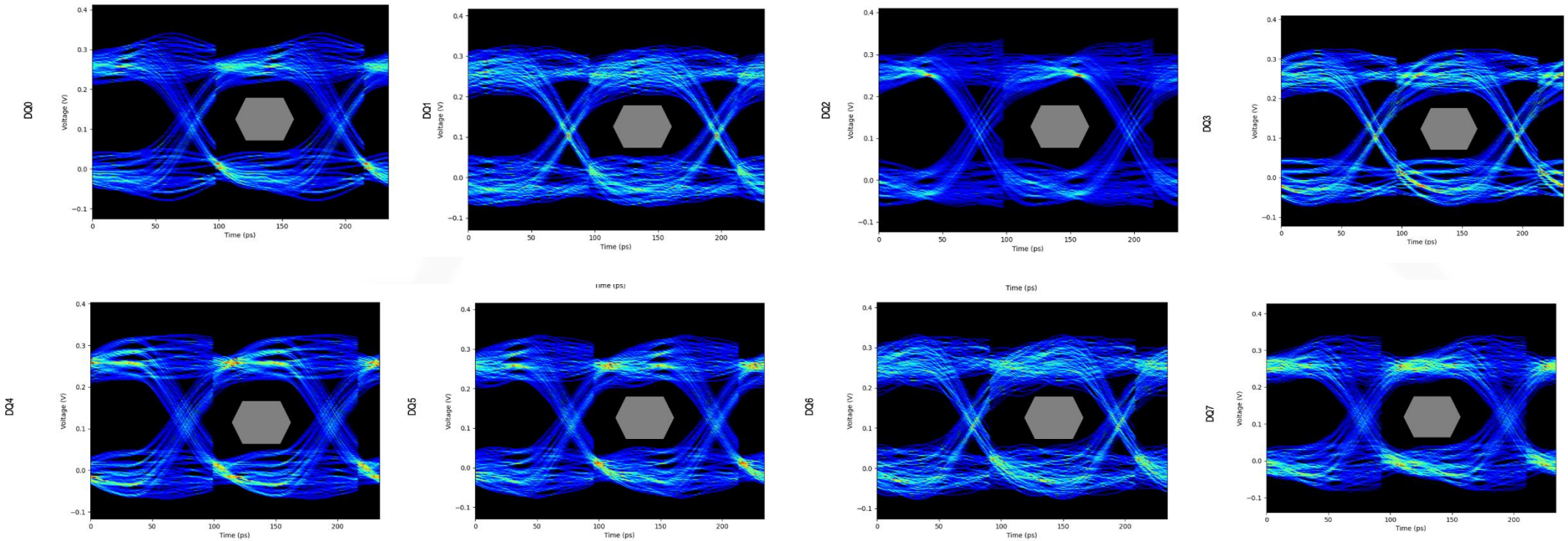


1. DFE is needed in links with a high-baud rate to min signal amplitude at high frequency caused by channel jitter.
2. Filter weights selected dynamically in a feedback loop to max eye opening.

Simulation Schematic



AMI Simulation Result



1. 1-tap DFE can help us achieve 8533Mbps rate design in the design of T3 PCB;
2. Multi-tap DFE can be used to further improve SI, but this must be weighed against increased power consumption, which is critical in low-power memory systems.

Thanks