KEYSIGHT

Chiplet Signal Integrity Simulation

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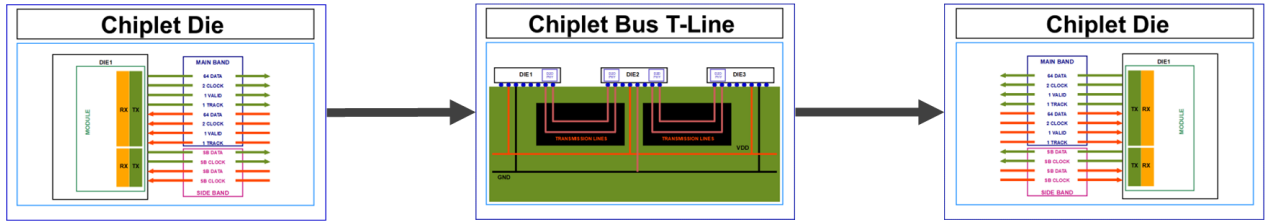
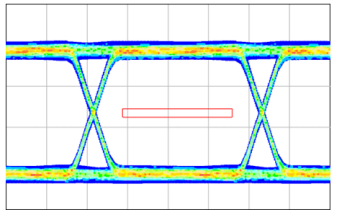
Agenda: Signal Integrity Journey in the UCIe Context

- **What is Chiplet**
- **Why is the industry shifting to the chiplet design philosophy**
- **Chiplet Simulate challenges**
- **Chiplet electrical layer simulation**

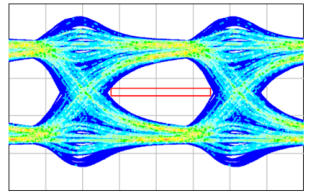
UCIe™
Universal Chiplet Interconnect Express

Electrical layer specifications
- Eye mask
- Equalization
- Loss and crosstalk level





Signal Integrity Insights on
- Crosstalk
- Frequency-dependent loss
- Equalization



What is Chiplet

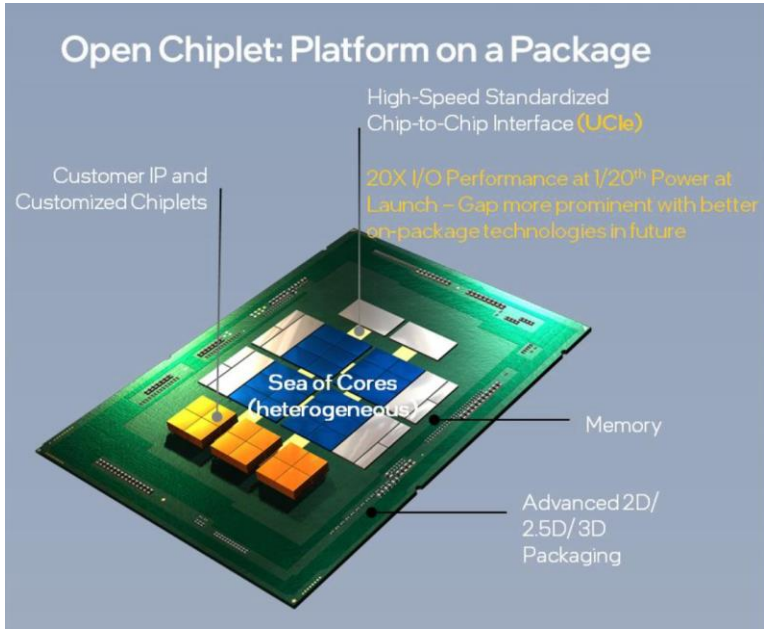
- A chiplet is an IC designed to be combined with other chiplets in a single package

- System on a single package rather than System on a Chip (SoC)
  - Avoiding one gigantic monolithic die by dividing it into several smaller dies and integrating them into a single package
  - Cost-effectiveness, power efficiency (lower picojoule/bit), improved thermal performance, higher yield, and faster development times
  - Similar to conventional SiP, SoP, PoP, PiP, etc., but with much higher-level integration based on advanced packaging technologies such as 3DIC and heterogeneous integration

- Multi-technology integration encompassing high-speed computing, RF, optics, etc

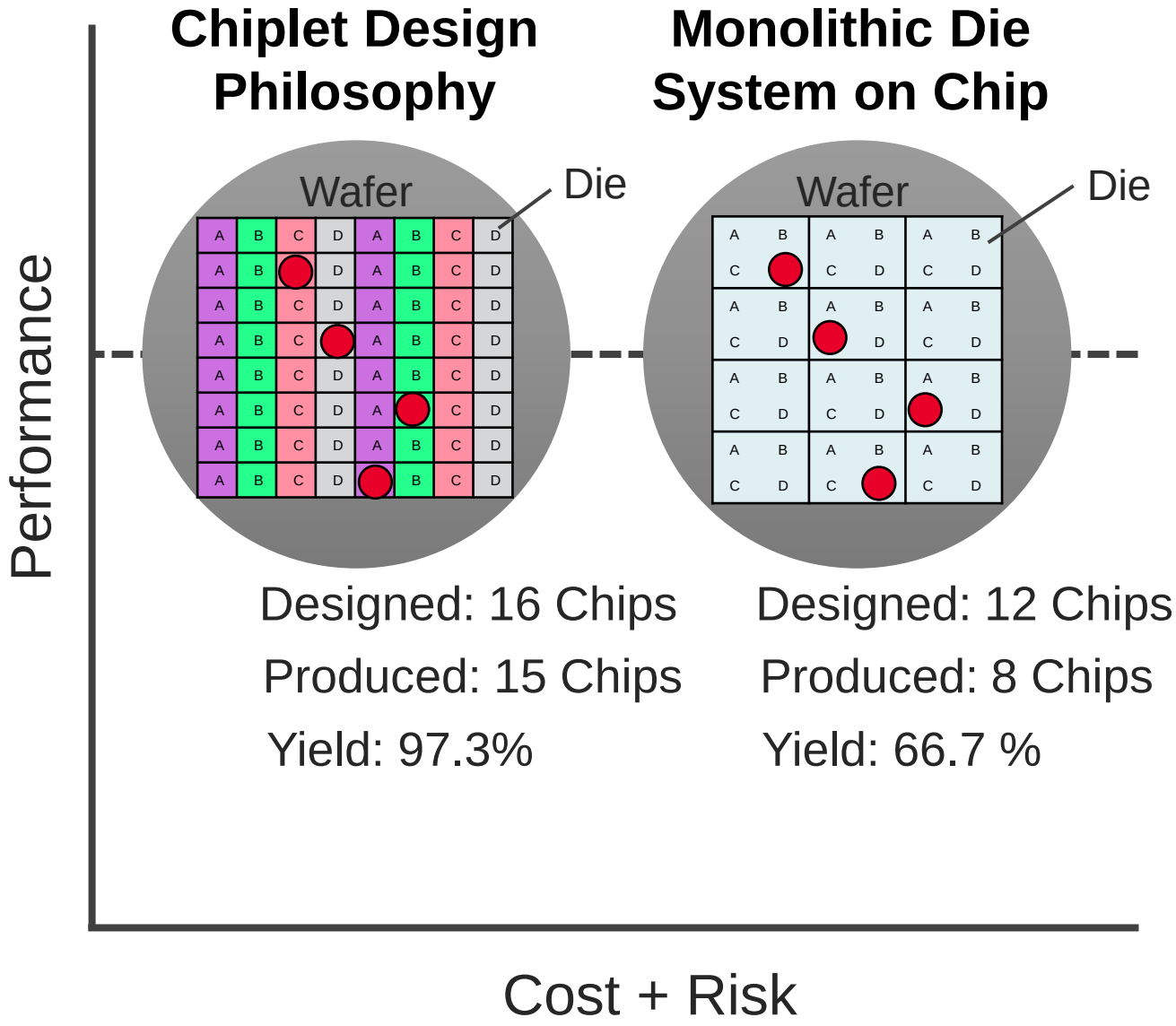
- Foundry-driven integration and standardization activities, such as TSMC 3DFabric and 3DBlox, are significantly shaping the landscape

- Wide reaching applications across various markets
  - Data centers and cloud computing
  - Telecommunications and networking
  - High performance computing (HPC)
  - Aerospace and defense
  - And more…



Source: UCIe Consortium

Chiplets Improve the Cost vs. Performance of Chip Production



Monolithic approach

4 different functions in one big die

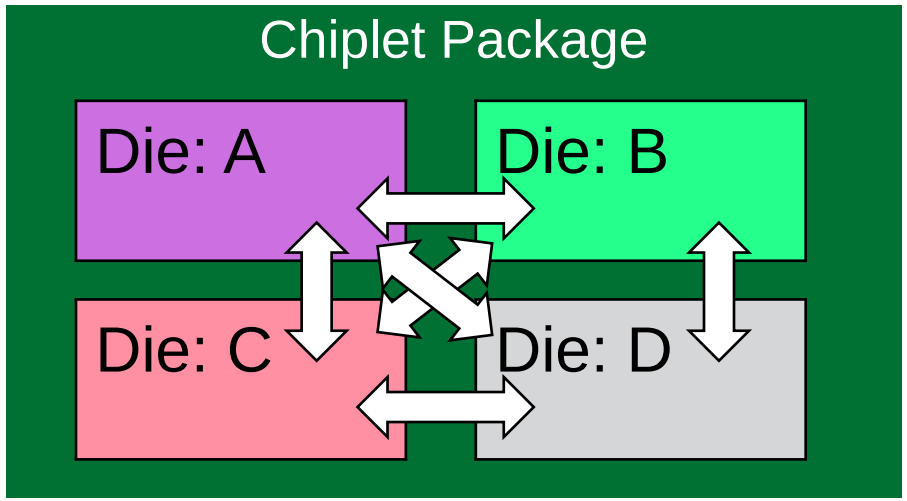
Fn: A (CPU)	Fn: B (Memory)
Fn: C (I/O)	Fn: D (Power)

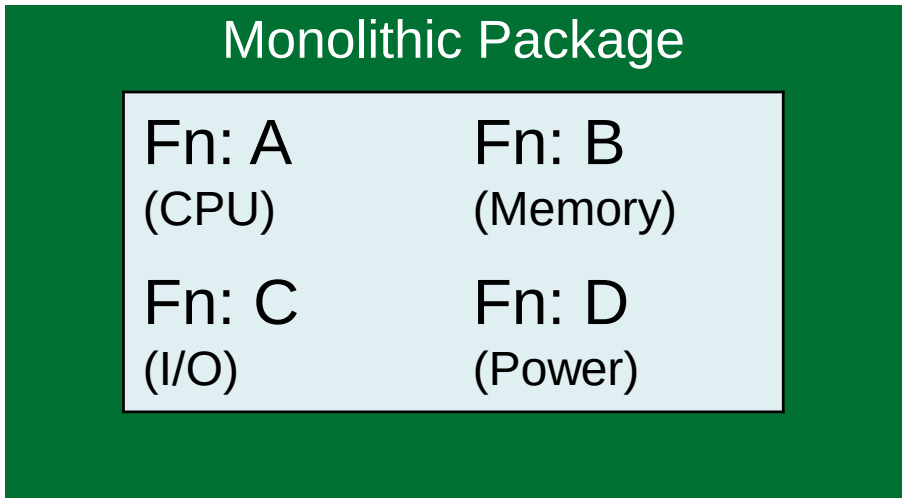
Chiplet approach

4 different dies for 4 different functions

Die: A	Die: B
Die: C	Die: D

The Catch: Die-to-Die Communication is Important for Chiplets



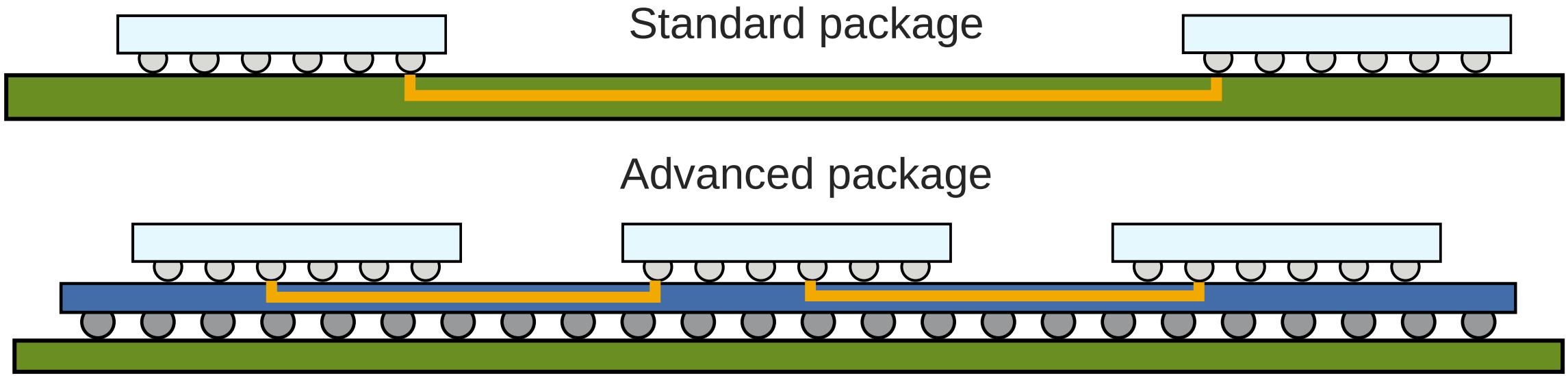


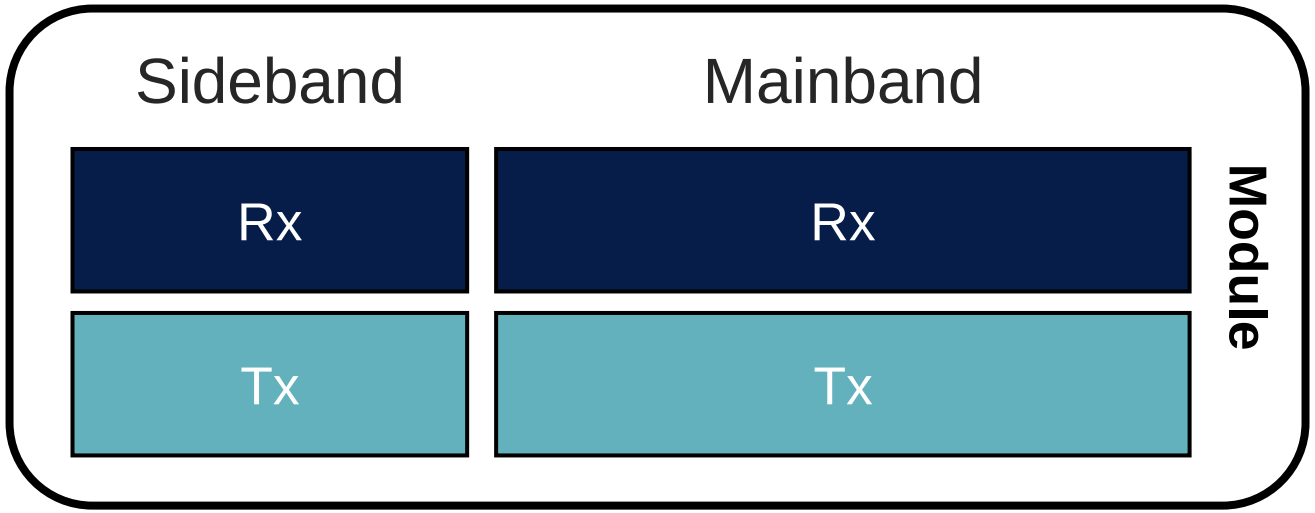
UCIe™
Universal Chiplet Interconnect Express

Various standards for the die-to-die interface between chiplets

- **UCIe (Universal Chiplet Interconnect express)**
- BoW (Bunch of Wires)
- AIB (Advanced Interface Bus)

UCIe Module and Data Rates for Std Pkg. and Adv. Pkg.



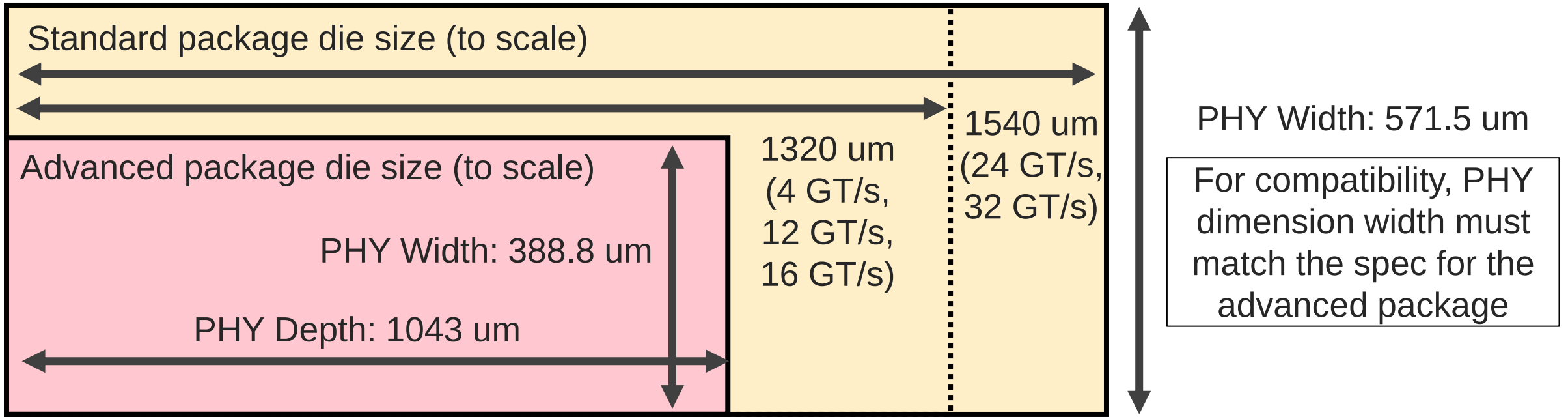


Data rate:

4 GT/s	8 GT/s	12 GT/s
16 GT/s	24 GT/s	32 GT/s

Standard Package and Advance Package Comparison

PHY dimension depth is an informative parameter and depends on bump pitch.

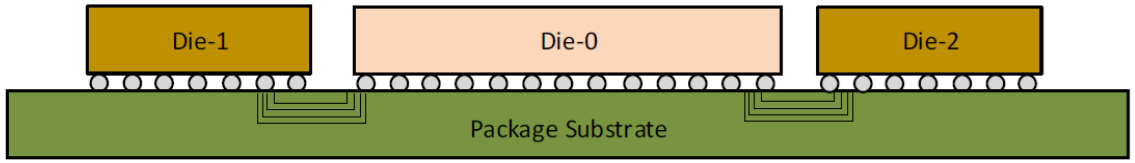


For compatibility, PHY dimension width must match the spec for the advanced package

Packaging	Bump Pitch	Channel Reach	Raw BER
Standard	100 um to 130 um	10 mm (Short reach) 25 mm (Long reach)	1e-27 (<= 8 GT/s) 1e-15 (>= 12 GT/s)
Advanced	25 um to 55 um	2 mm	1e-27 (<= 12 GT/s) 1e-15 (>= 16 GT/s)

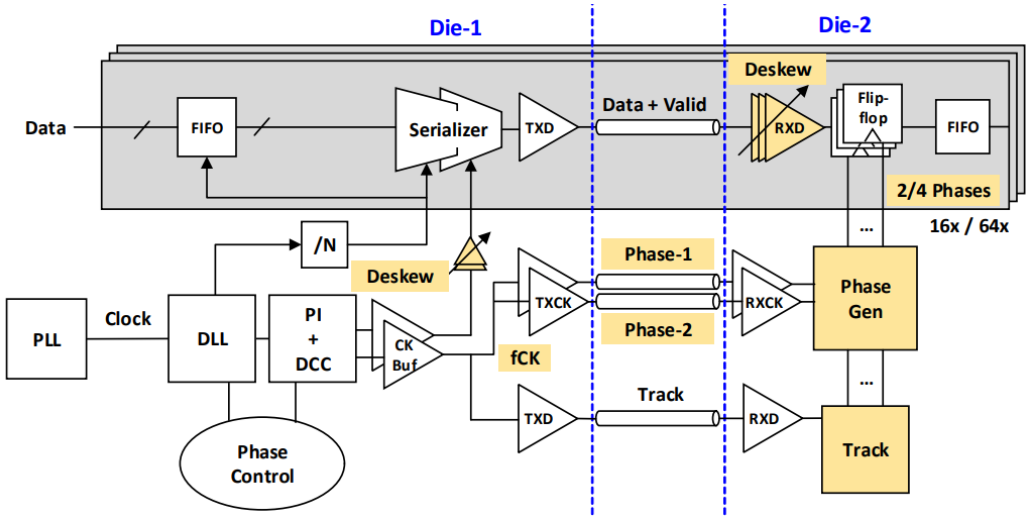
Signal Integrity Challenges

- Data is single-ended signal
- Handles different rising and falling edge rates for Single-Ended signals
- Rigorous statistical calculations for Data eye probabilities at arbitrarily low BER
- Check eye contours at target BER ($<10^{-15}$ or $<10^{-27}$) against Data mask
- Account for crosstalk between all signal lines
- Measurements: Eye height, Eye width, Triggered Eye, contour, BER, VTF (Voltage Transfer Function), etc
- Single-end IBIS-AMI modeling and simulation

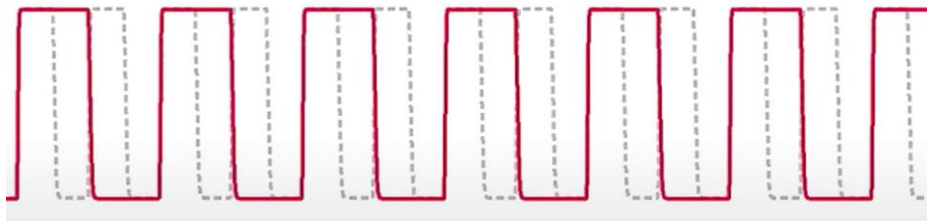


UCIe Clock

- Each module supports a two-phase forwarded clock.
- Per-Lane Deskew must be supported on the Transmitter at high data rates.
- The Receiver must provide matched delays between the Receiver clock distribution and Data/Valid Receiver path.
- Transmitter must support quadrature phases in addition to differential clock



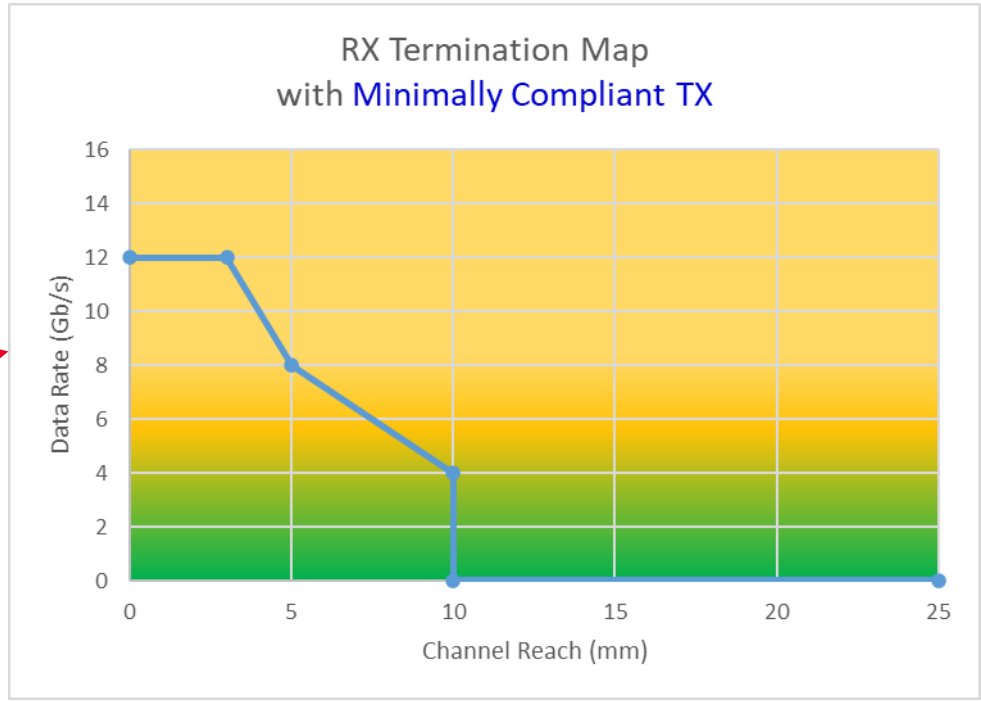
Data rate (GT/s)	Clock freq. (fCK) (GHz)	Phase-1	Phase-2	Deskew (Req/Opt)
32	16	90	270	Required
	8	45	135	Required
24	12	90	270	Required
	6	45	135	Required
16	8	90	270	Required
12	6	90	270	Required
8	4	90	270	Optional
4	2	90	270	Optional



Termination

- Advanced Package
  - Up to 2mm and 32Gb/s, TX drive control.
  - No RX Termination

- Standard Package
  - TX Termination
  - RX Termination Map



Voltage Transfer Function (VTF) Based Metrics

- Voltage Transfer Function (VTF) based metrics are used to define insertion loss and crosstalk.

Loss

- Loss is defined as the ratio of the receiver voltage and source voltage

$$L(f) = 20\log_{10}|V_r(f)/V_s(f)|$$

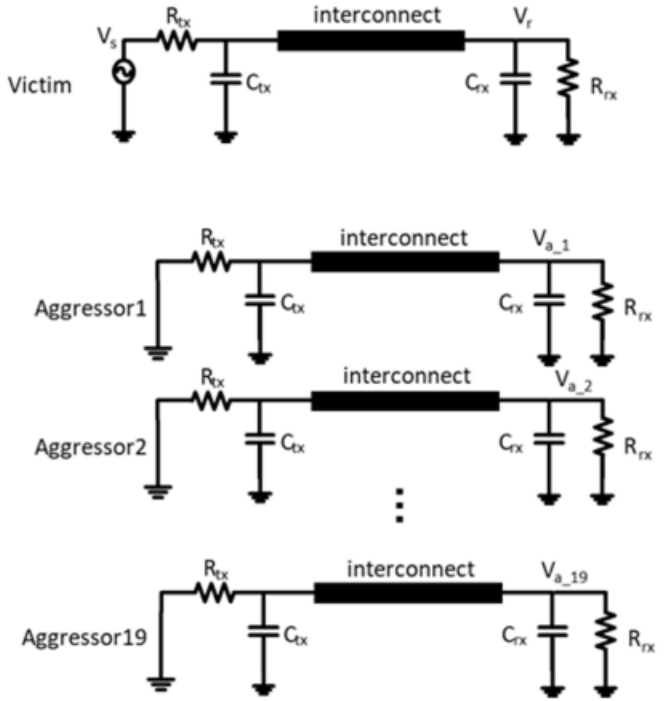
$$L(0) = 20\log_{10}\left(\frac{R_{rx}}{R_{tx} + R_{channel} + R_{rx}}\right)$$

- $L(0)$ is 0 for unterminated channel

Crosstalk

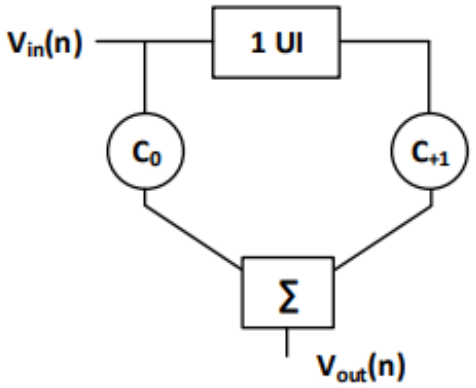
- 19 aggressors included
- Crosstalk is defined as the power sum of the ratios of the aggressor receiver voltage to the source voltage
- Based on crosstalk reciprocity

$$XT(f) = 10\log_{10}\left(\sum_{i=1}^{19}\left|\frac{V_{a\_i}(f)}{V_s(f)}\right|^2\right)$$



Tx AMI

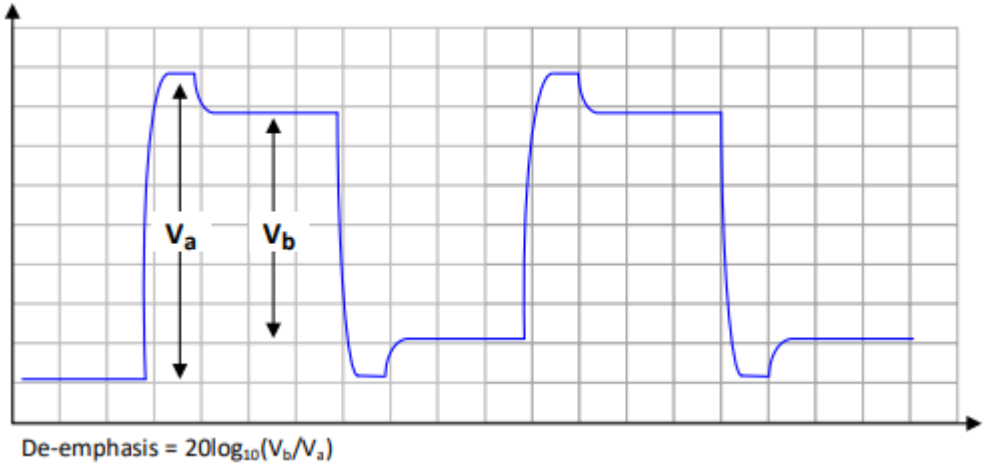
- Transmitter equalization is recommended for 16 GT/s and must be supported at 24 GT/s and 32 GT/s data rates to mitigate the channel ISI impact.
- Tx equalization is de-emphasis only for all applicable Data rates.



$$V_{out}(n) = C_0 V_{in}(n) + C_{+1} V_{in}(n-1) + |C_{+1}|$$

$$|C_0| + |C_{+1}| = 1$$

$$V_{in}(n) = \{0, +1\}$$



Setting	De-emphasis	Accuracy	C_{+1}	V_b/V_a
1	0.0 dB	-	0.000	1.000
2	-2.2 dB	+/- 0.5 dB	-0.112	0.776

Rx AMI

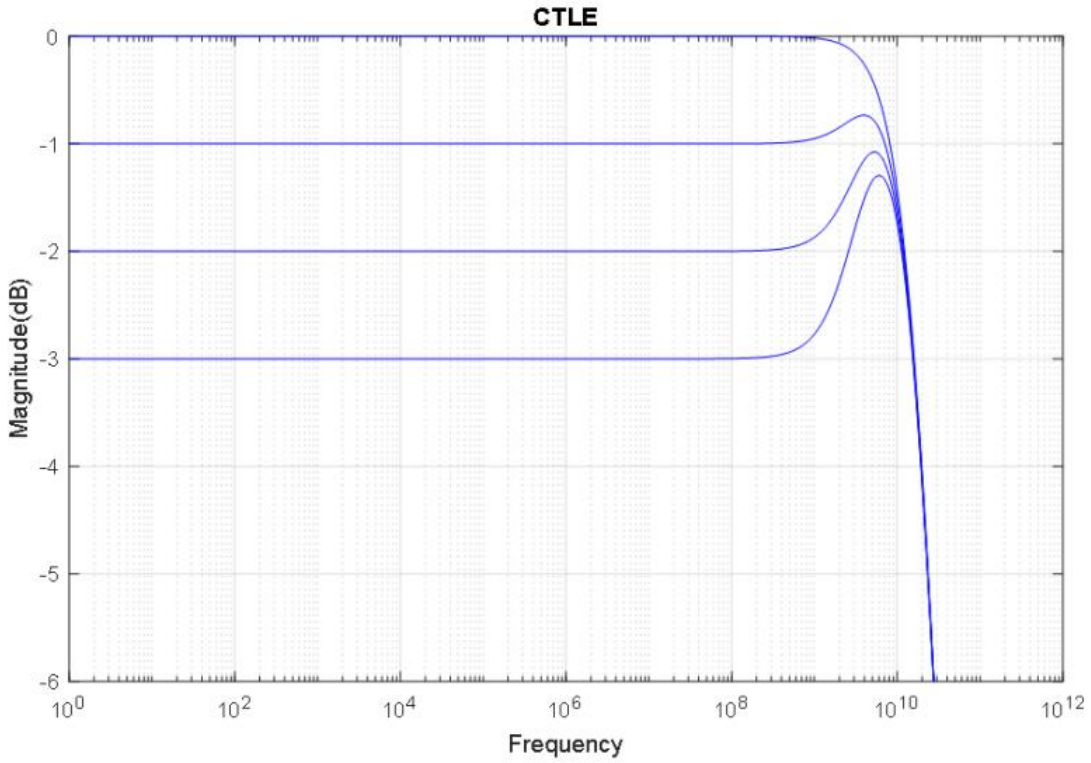
- Receiver equalization may be implemented at 24 GT/s and 32 GT/s data rates.
- Implementation can be CTLE, inductive peaking, 1-tap DFE, or others. Expected RX equalization capability is equivalent of 1st order CTLE.

$$H(s) = \omega_{p2}\left(\frac{s + A_{DC}\omega_{P1}}{(s + \omega_{p1})(s + \omega_{p2})}\right)$$

$$\omega_{p2} = 2\pi * DataRate$$

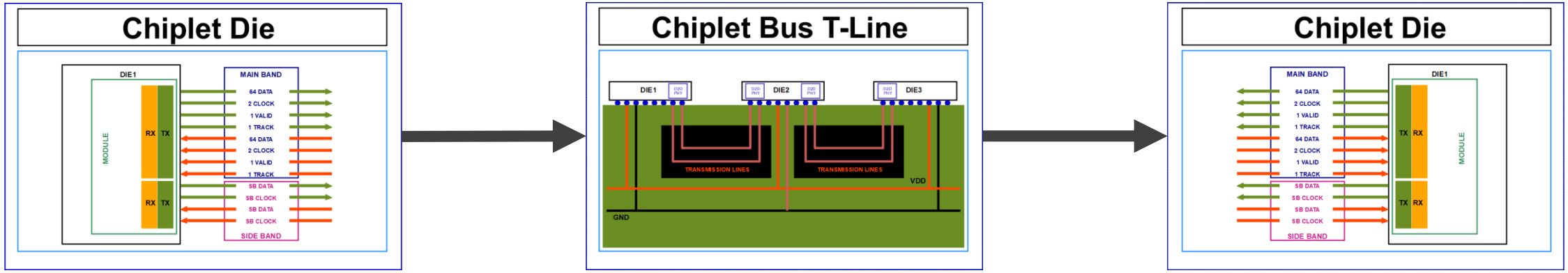
$$\omega_{p1} = 2\pi * DataRate/4$$

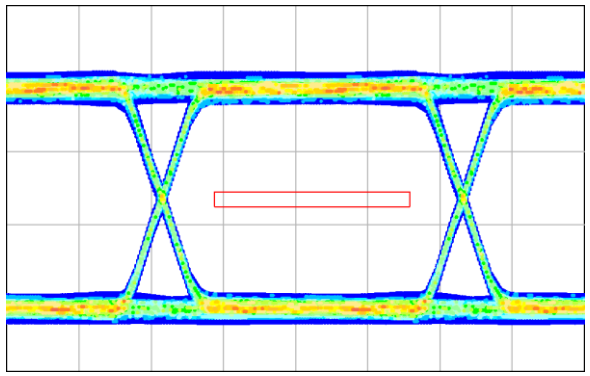
$$A_{DC} = DC\ Gain$$



How to Simulate Chiplet?

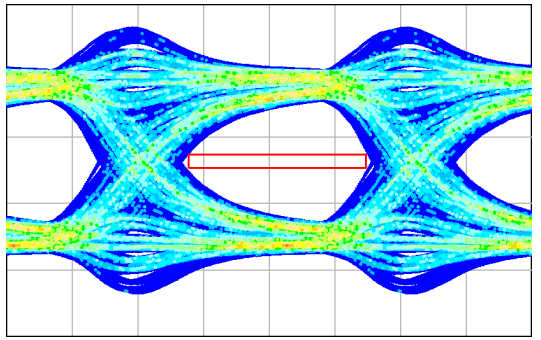
Std Pkg UCIe Link Example with Signal Integrity Insights





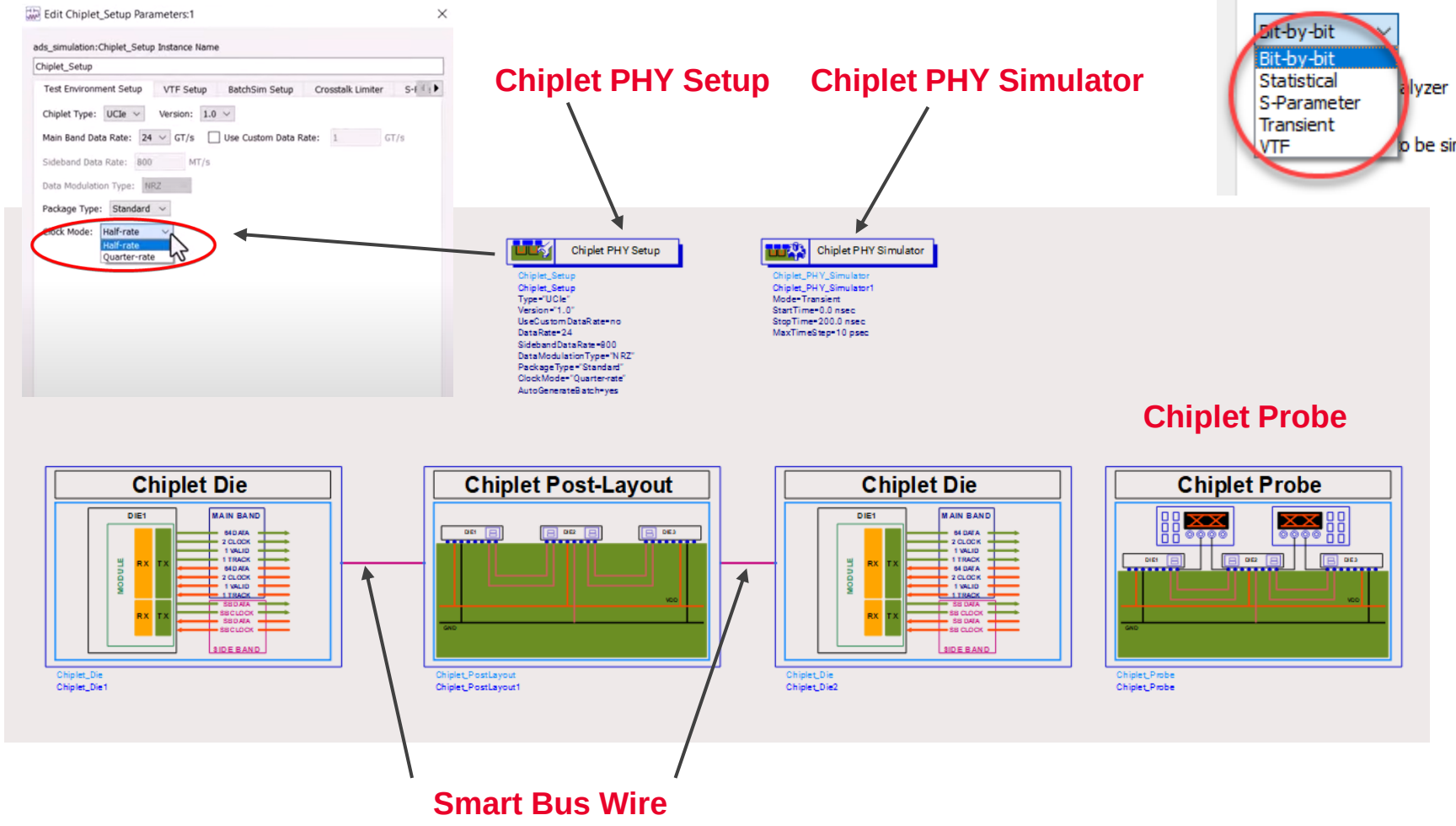
Signal Integrity insights on

- Crosstalk
- Frequency-dependent loss
- Equalization

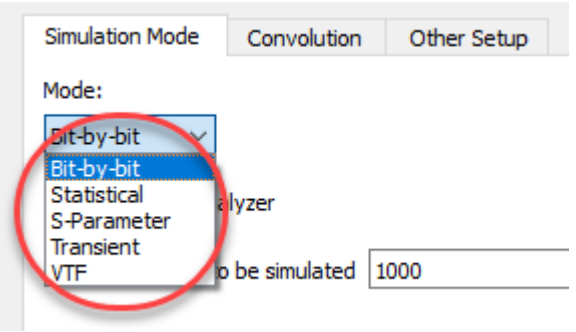


Chiplet Simulation

Smart Design Environment



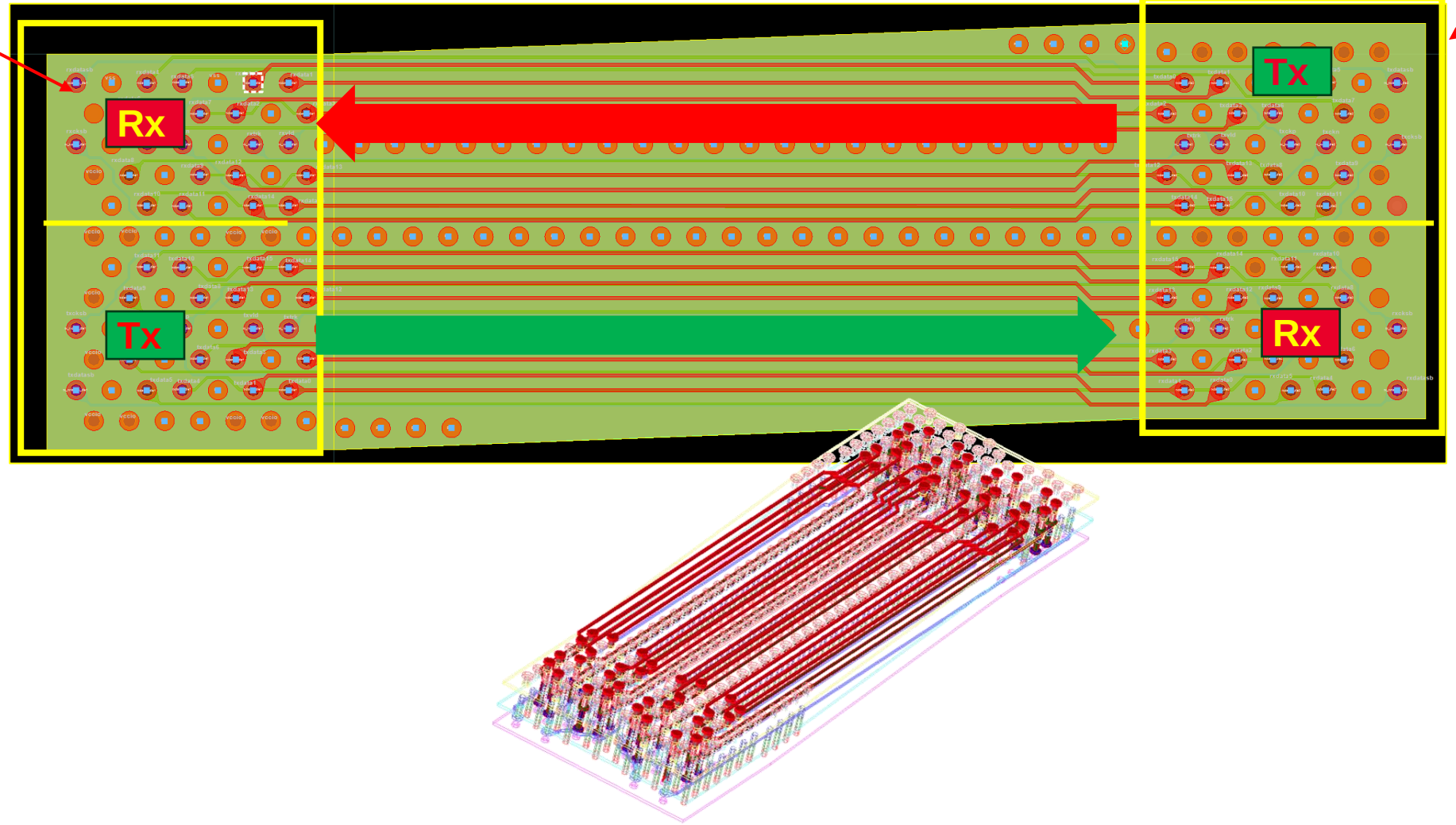
Simulation Mode



Chiplet Simulation- Package Simulation

A sample design example with Standard Package

Chiplet
D2D PHY
Ball Map
(Module)



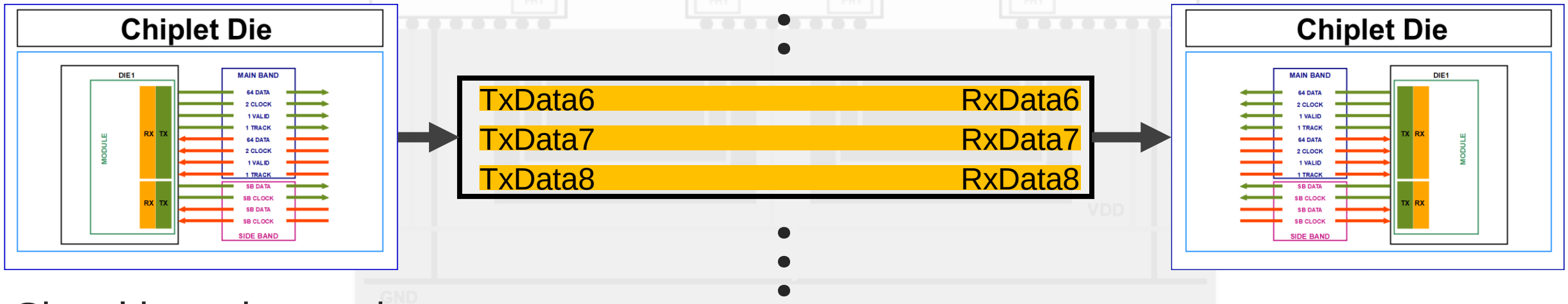
Chiplet
D2D PHY
Ball Map
(Module)

Chiplet Channel Simulation

Standard Package
Data rate: 24 GT/s

20 transmission lines

Rx Termination
50 Ω



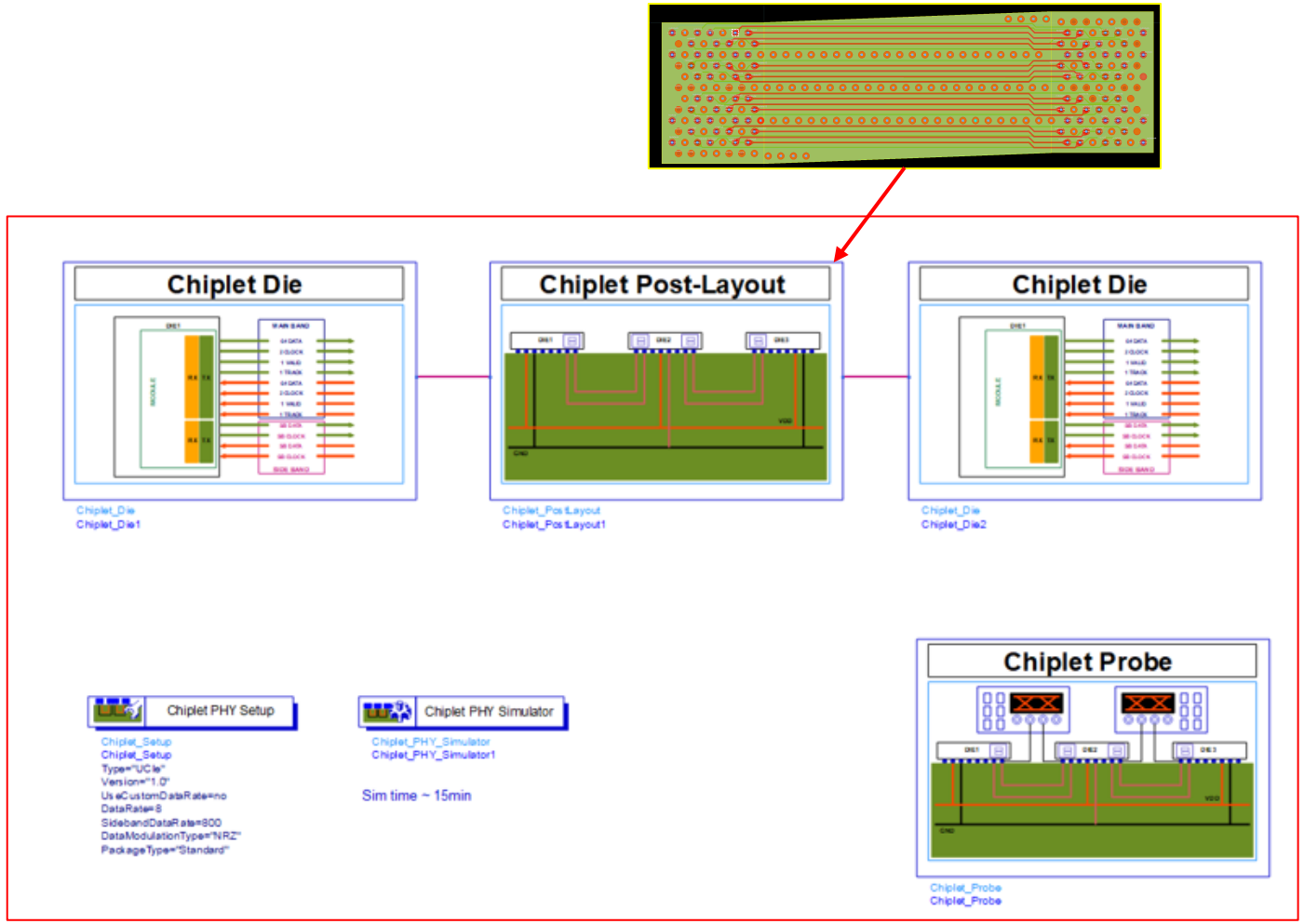
Signal integrity metrics
- Tx Eye diagrams

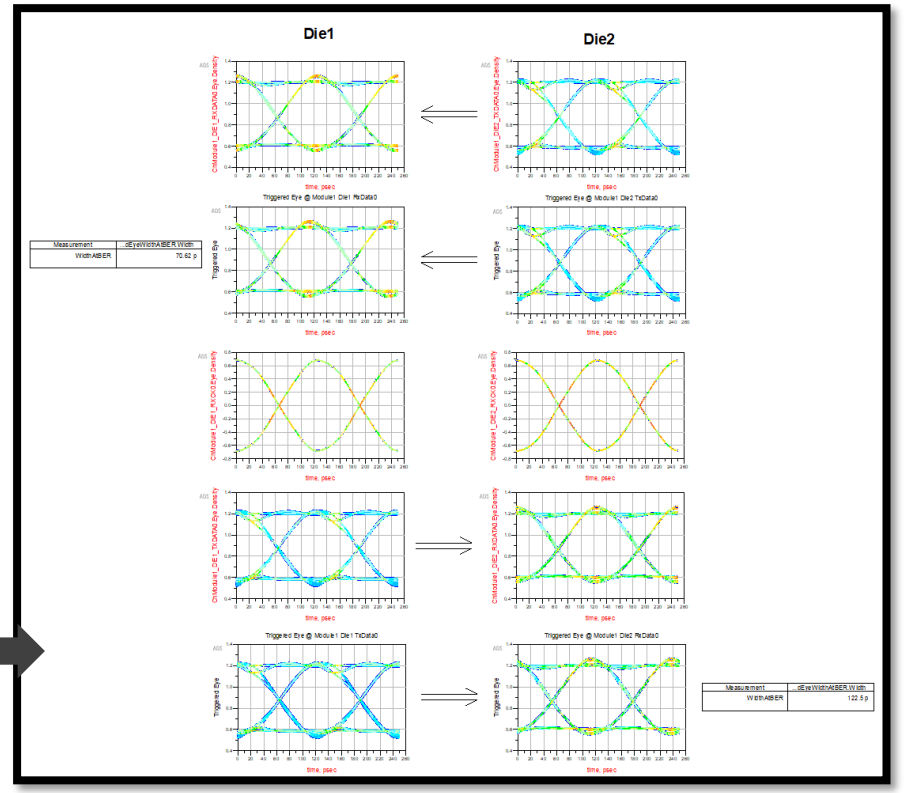
Signal integrity metrics
- VTF loss
- VTF crosstalk

Signal integrity metrics
- Rx Eye diagrams

Chiplet Simulation– Simulation Example for Eye, BER, Contour

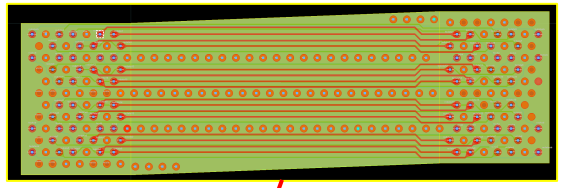
Using Chiplet PHY Simulator with Bit-by-Bit Mode

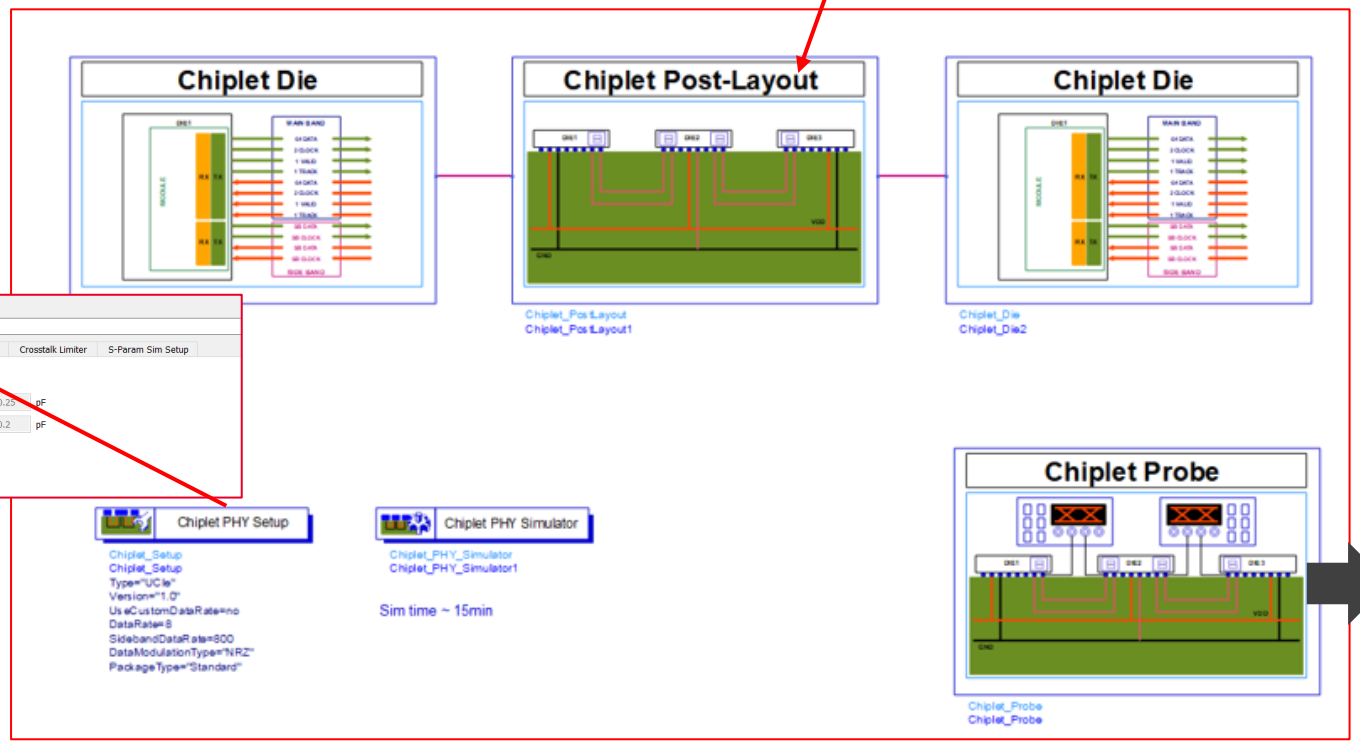


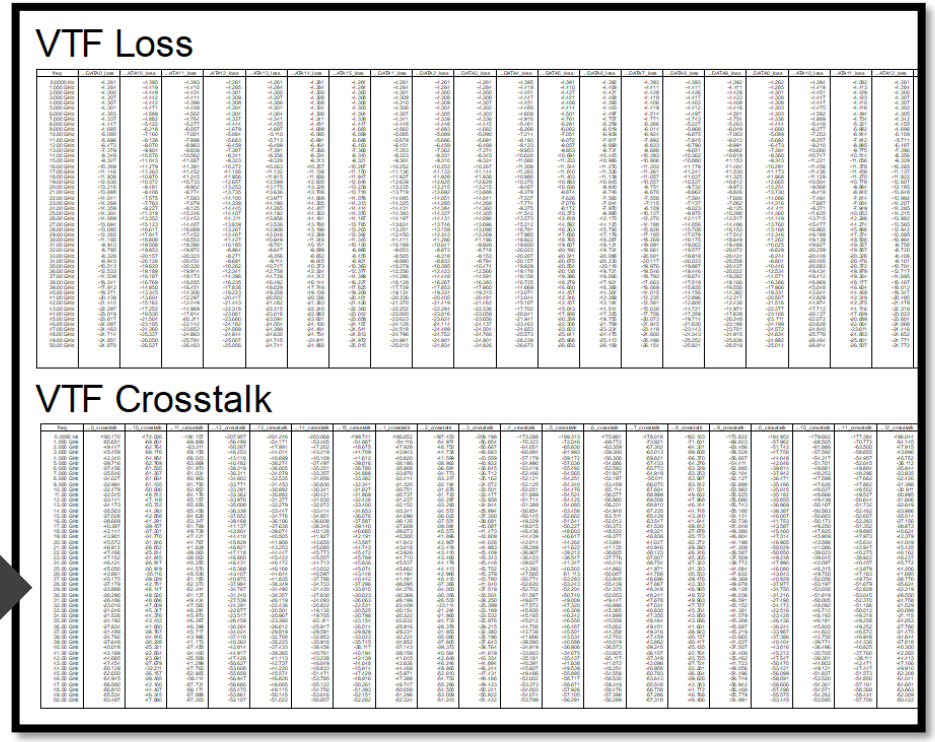


Chiplet Simulation– VTF Simulation

Using AC Simulator with BatchSim

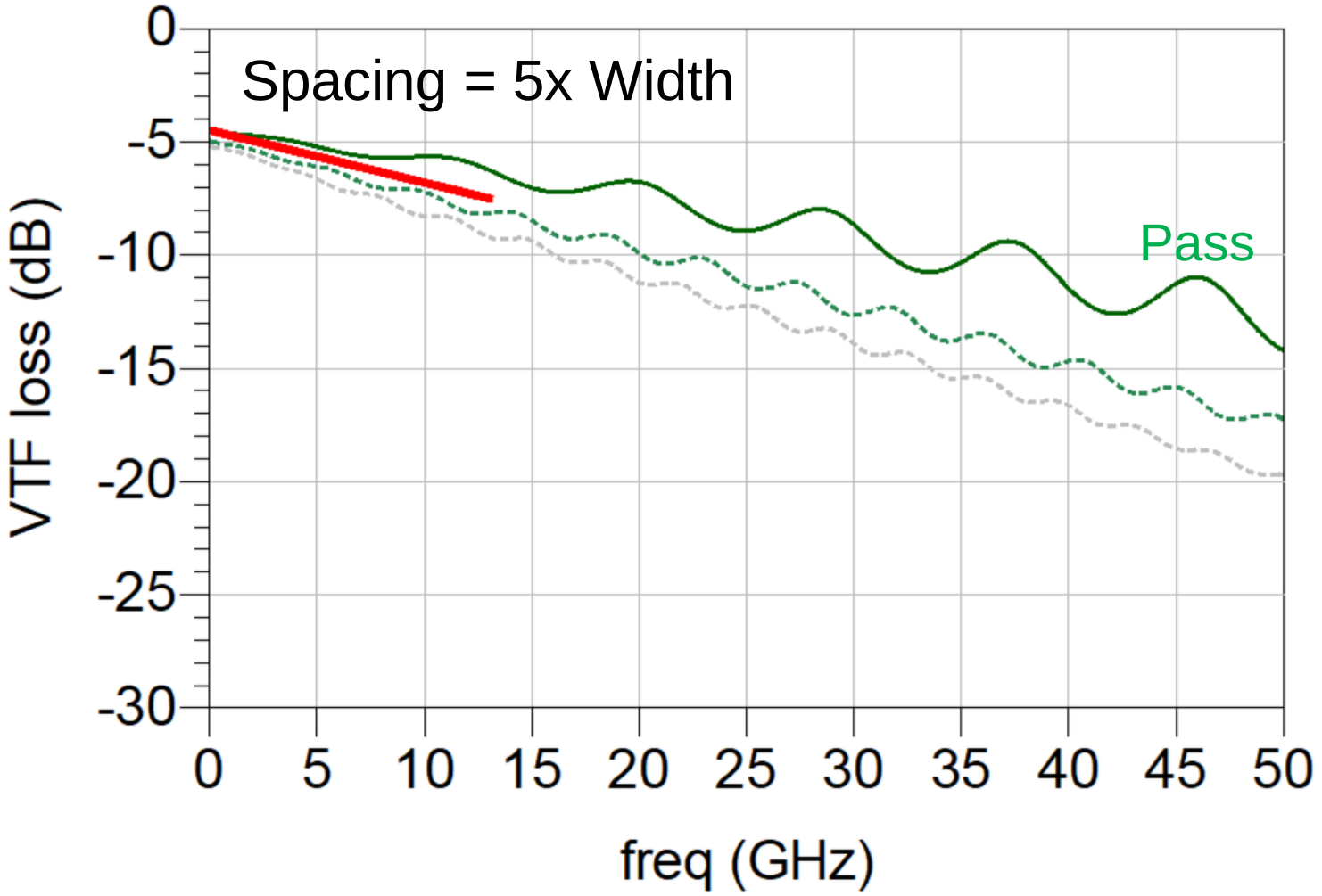






Case: Shorted the Length to Reduce Loss and Pass the Line

For the current material configuration, we can only afford a short-reach channel.

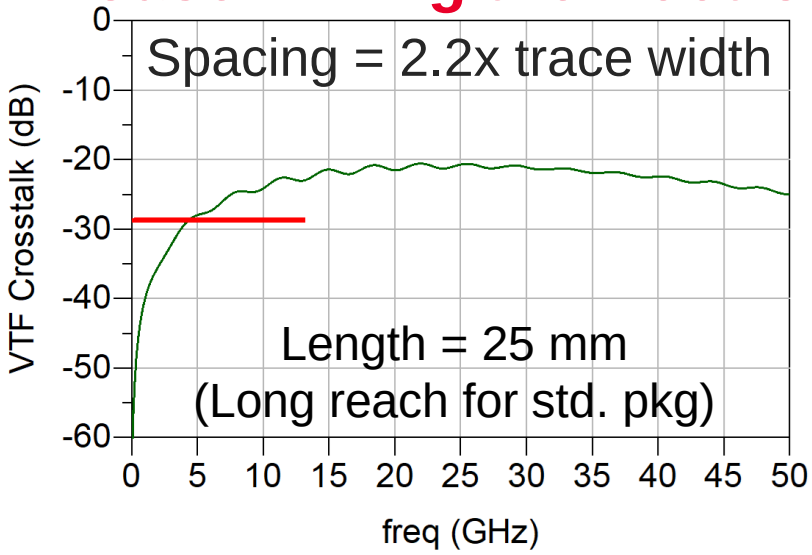


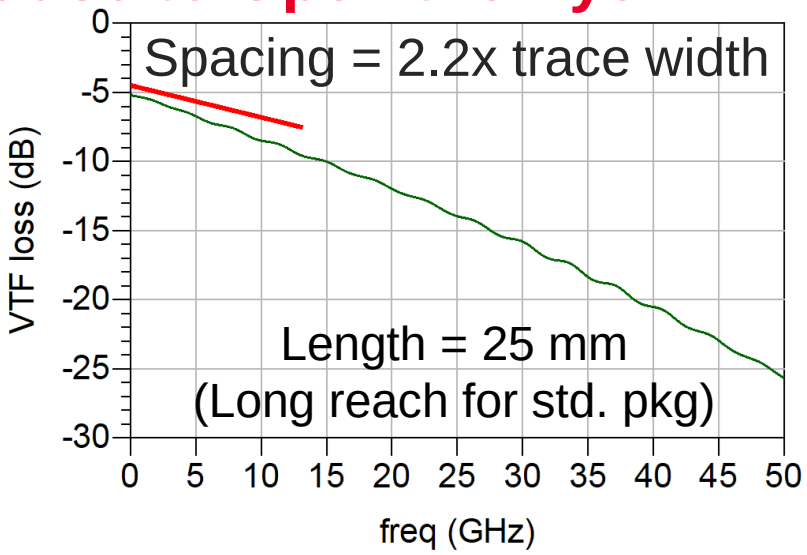
(Short reach for std. pkg)
Length = 10 mm

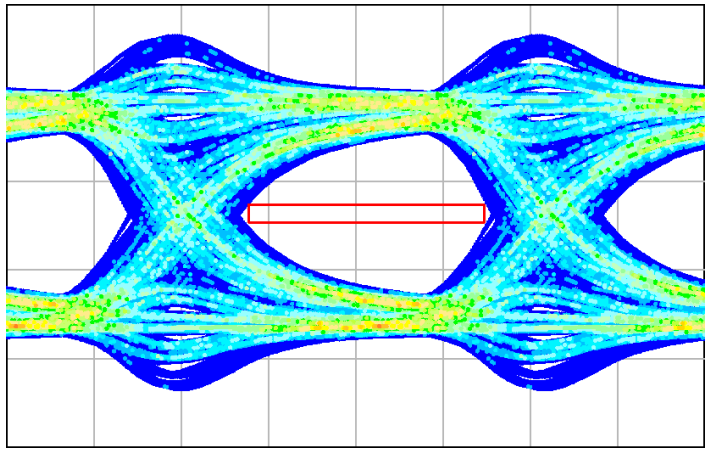
Length = 20 mm

Length = 25 mm
(Long reach for std. pkg)

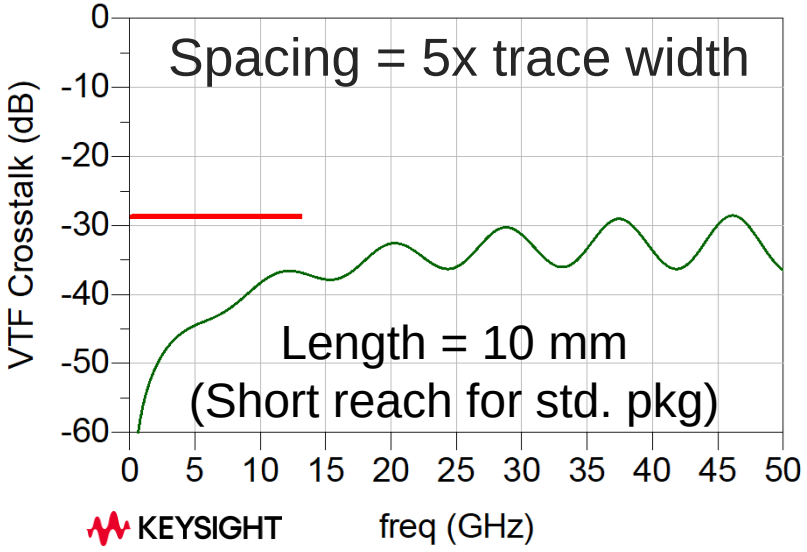
Case: Fixing the Root Cause to Open the Eye

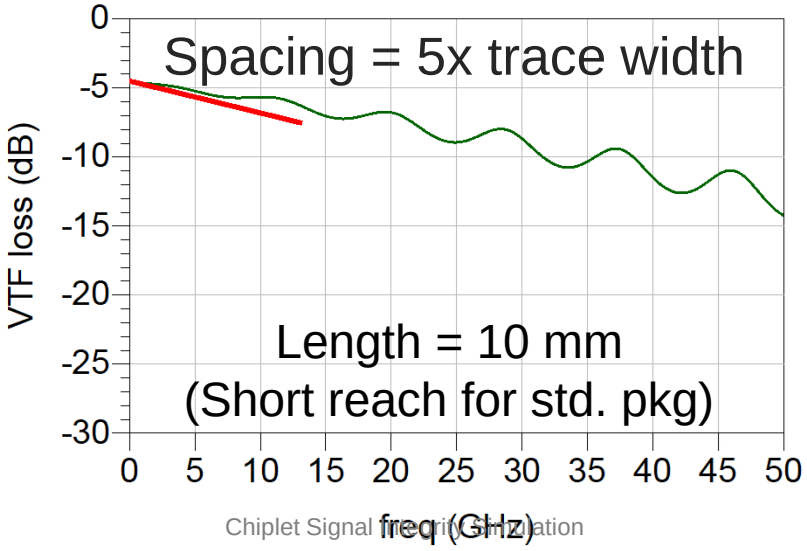


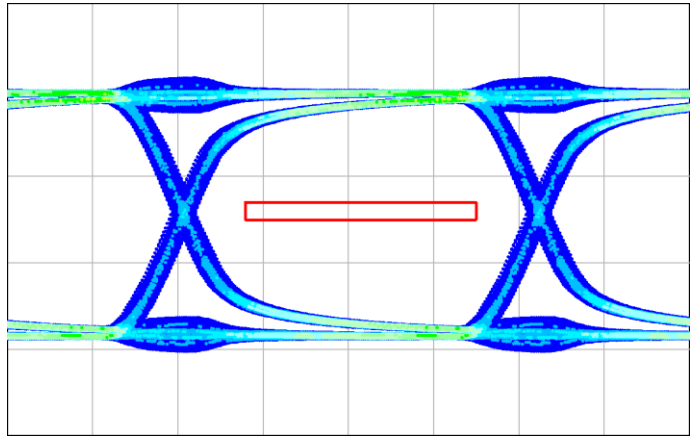




The eye is open after we reduced the root causes, the coupling and loss.



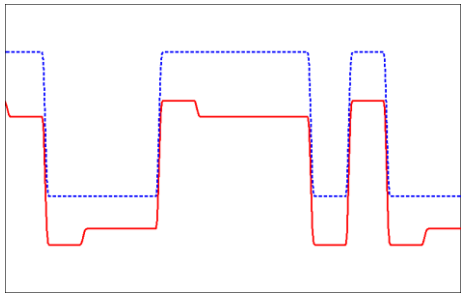


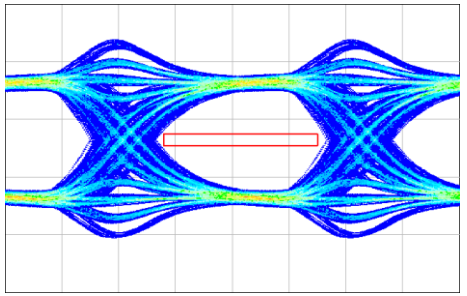


Key Attributes to a Chiplet D2D Comm. SI Analysis

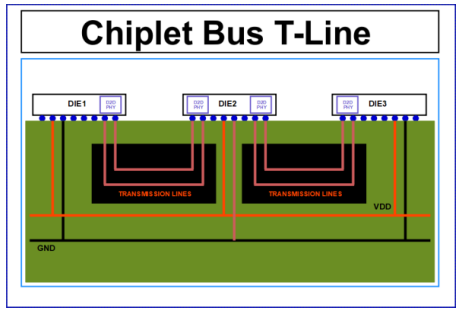
Standard-focused
Let the software work for you

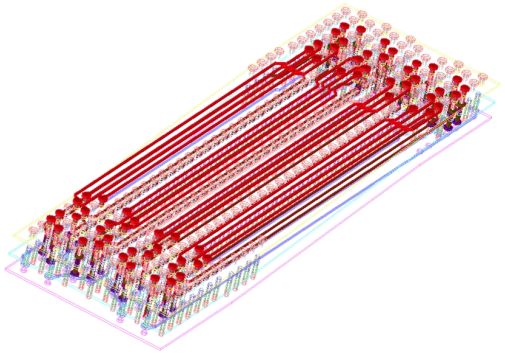
Tx and Rx Termination and Equalization
Explore possible design and solution space



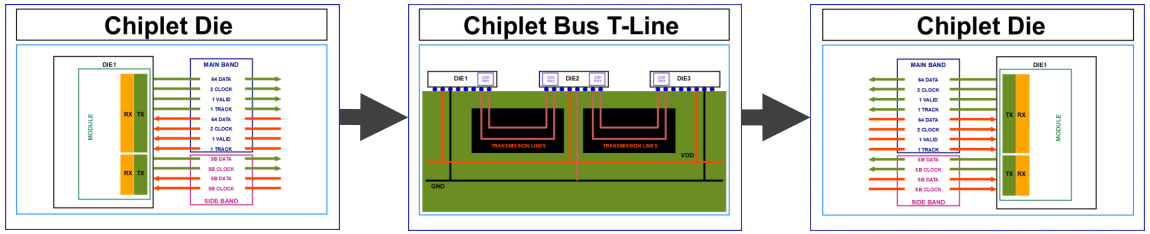


Die-to-Die Interconnect Extraction and Modeling
Understand design space and validate design choices





Die-to-Die Channel Link
Identify problem early, reproduce existing problem

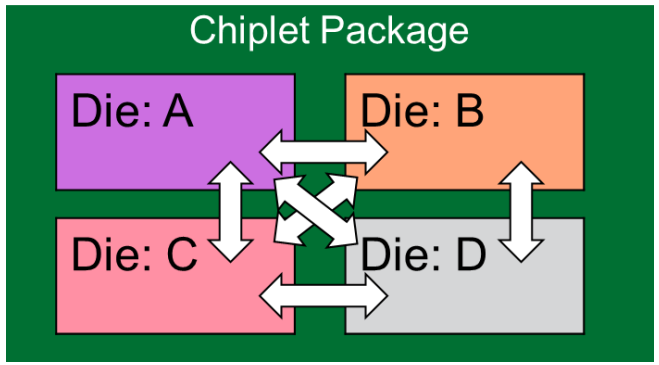


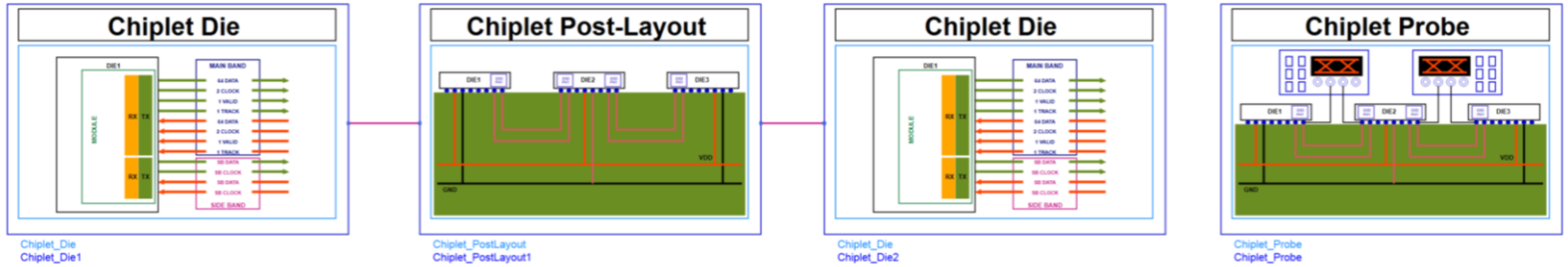
Usability and Integration
Don't work for the computer

Summary

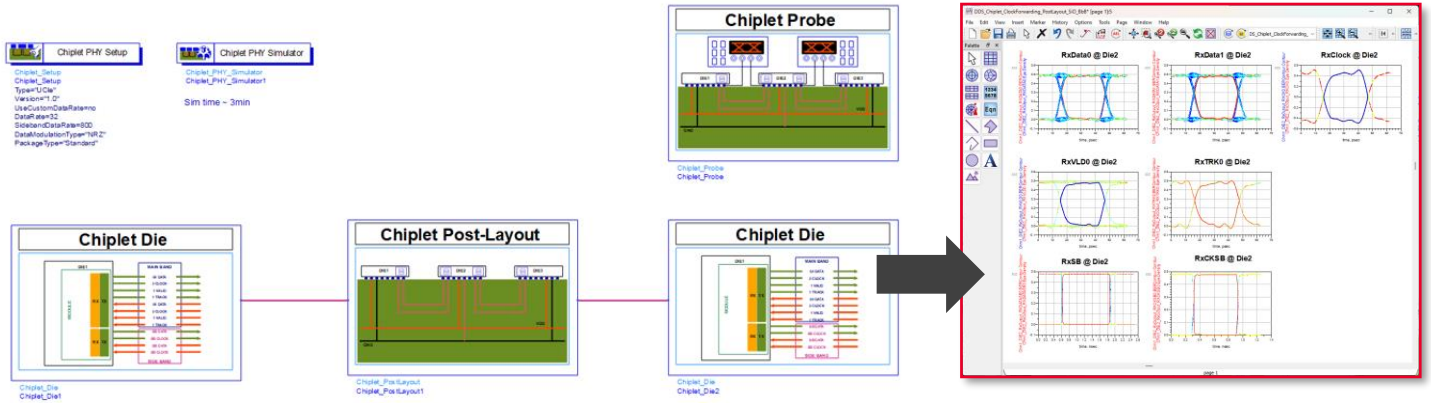
Chiplet Simulation

It is very important to analyze chiplets from D2D to D2D at a system level using smart design environment, it can help engineers find and solve problems as quickly as possible.

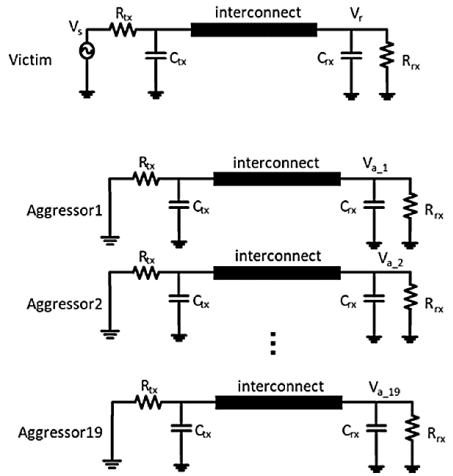




Supports differential **forwarded clock** in UCIe, BoW, AIB standard.



Standard Driven VTF Measurements



KEYSIGHT

Thank you