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A Review of existing Multi-Gbps Serial Channel Analysis Methods and the Evolution of the Proposed IBIS ATM Algorithmic Modeling Standard

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Introduction

The IBIS Advanced Technology Modeling (ATM) committee has a proposal for a flexible approach to system level modeling of multi-Gbps channels

The principal target for this modeling technology is the PCB system designer

Other standards bodies such as the IEEE and INCITS have undertaken major efforts to define standards for multi-Gbps channels

This includes standardized modeling for these channels, principally targeted at the IC designer

This paper contrasts the modeling approaches and shows how the IBIS ATM proposal promises to solve problems not addressed by previous solutions

It also suggests how some of the features of previous approaches could be incorporated into the IBIS ATM proposal at future date.

Overall goal – Design and implement reliable 1-10Gbps self clocked serial channels

The Silicon Vendor

Design Transmitter and Receiver meeting specified channel standard and BER

- **Must be interoperable with other vendors designs for that channel standard e.g. 802.3ap and CEI11**

Simulate Transmitter, Receiver and representative interconnect

Create Prototype silicon and PCB, measure actual performance

- **Silicon design must tolerate a range of real PCB channel layouts with connectors, vias and cables**

Correlate simulation results to measurements to fine tune the modeling process

The PCB System Implementer

Choose IC vendors and technology

Plan channel implementation: set constraints on layers, lengths, via types

Simulate Transmitter, Receiver with representative interconnect

Layout channel, re-simulate with accurate modeling of channel

Fabricate PCB, measure actual performance

Correlate simulation results to measurements to fine tune the modeling process

Distribution of multi-Gbps models from the IC vendor to the PCB systems implementer

In creating models, the IC vendor wishes to satisfy customers while:

Protect their intellectual property

Delivery accurate, easy to use models that require a minimum of support

Minimize the incremental cost in providing externally distributed models

The PCB System Implementer has additional preferences:

Compatibility of models between IC vendors and support from multiple SI analysis tools

Simulation speeds that allow full coverage of a design including corner case analysis

This presents new model creation challenges for the IC vendor

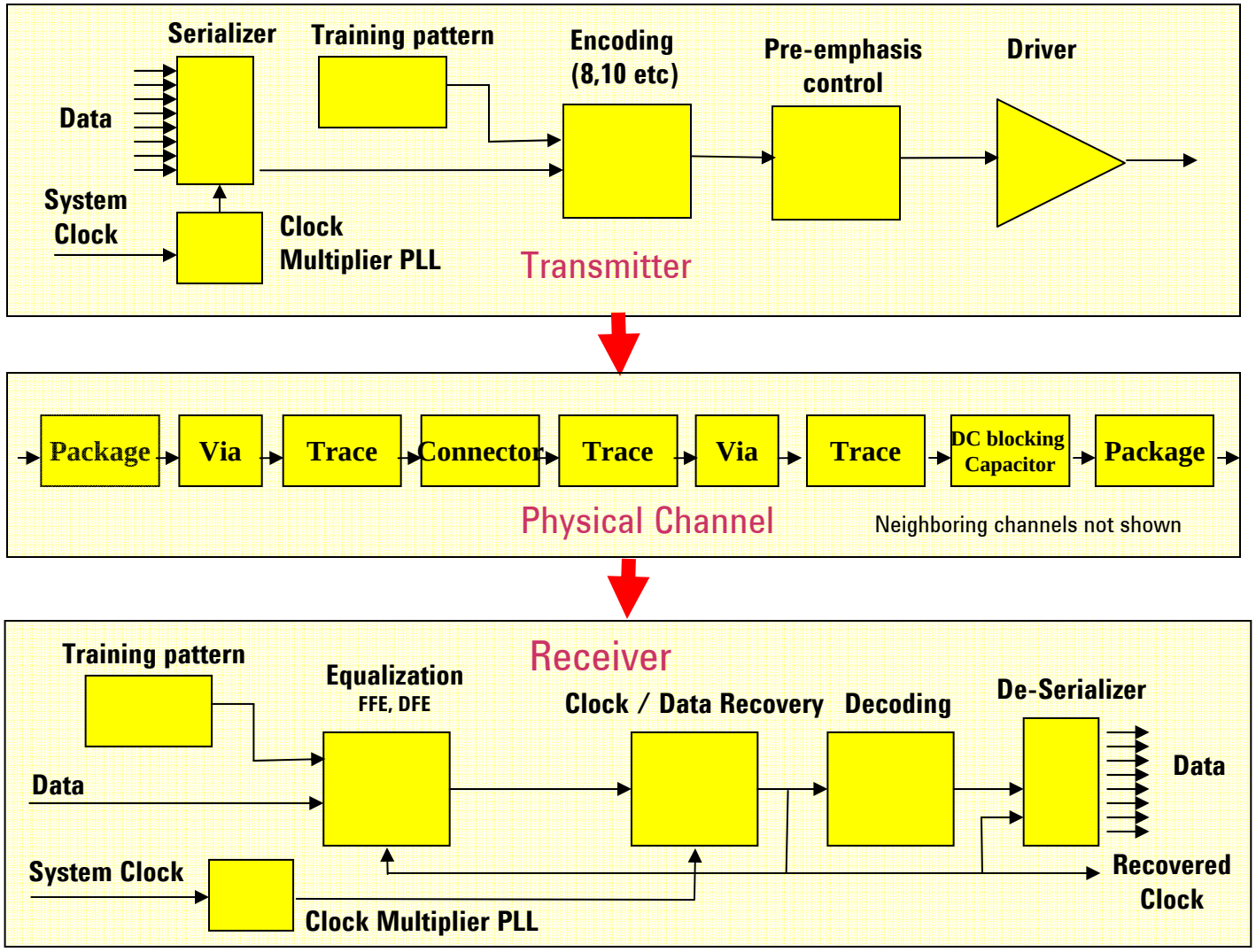
Historically many IC vendors internally utilized SPICE to design their general purpose buffers

IBIS was the preferred format for model distribution, frequently created from the IC vendors internal SPICE models using SPICE to IBIS utilities

Some IC vendors preferred to delivered encrypted versions of their internal SPICE models.

Today IC vendors are internally using a mixture of SPICE, RTL and system level tools to design multi-Gbps buffers and the channel control logic

The topology of a typical 6 Gbps serial channel



Approaches to multi-Gbps simulation

Transistor and circuit level

Drivers and receivers are modeled using SPICE, IBIS and SPICE macro-models

Packages and interconnect are modeled using transmission line and 'S' parameter models

Minimize the incremental cost in providing externally distributed models

Good accuracy but poor simulation speed

Circuit and system level co-simulation

Drivers and receivers are modeled using IBIS and SPICE macro-models co-simulating with RTL, Verilog AMS, VHDL-AMS, System-C, Proprietary 'C' or 'C++" and system level simulation tools.

Packages and interconnect are modeled using impulse response, transmission line and S-parameter models

Good accuracy and moderate simulation speed

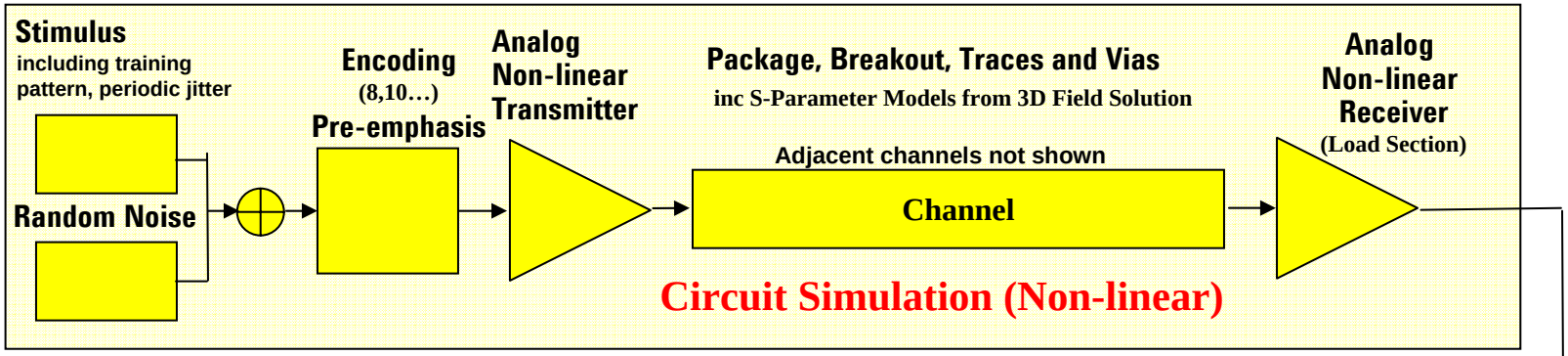
System level simulation

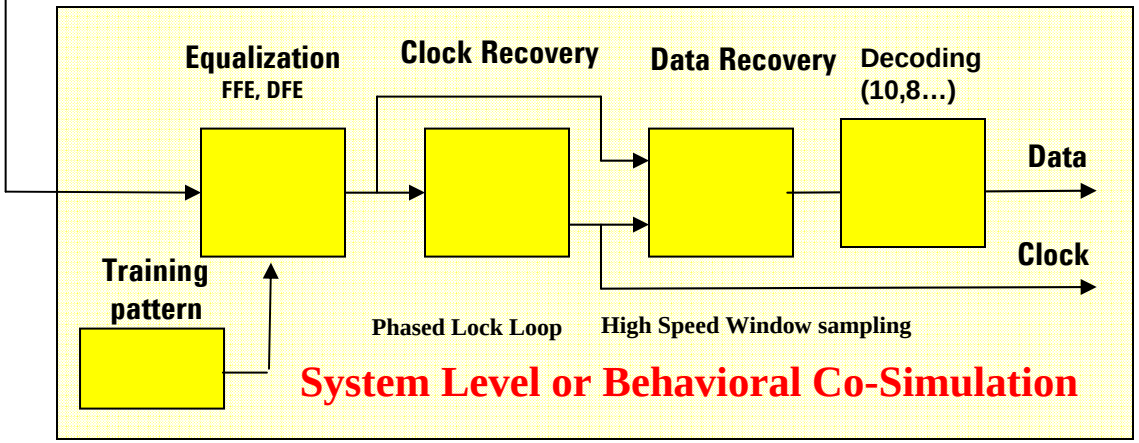
Drivers and receivers are modeled using RTL, Verilog AMS, VHDL-AMS, System-C, Proprietary 'C' or 'C++" and system level simulation tools.

Channels are characterized using impulse response or S-parameter models

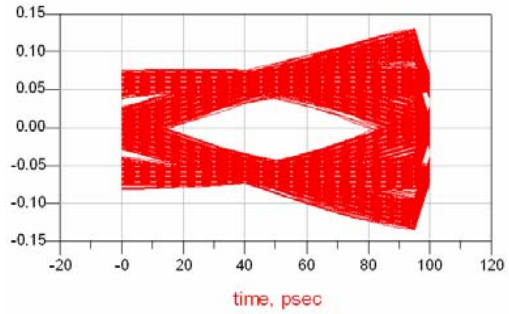
Moderate Accuracy with good simulation speed

Circuit and system level co-simulation of a multi-Gbps channel

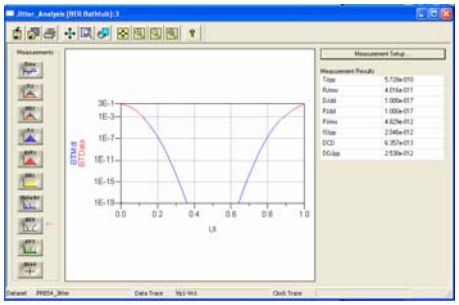




Recovered Data Eye Diagram
(includes periodic and random jitter)



Jitter/BER Plots



Random Noise Extrapolation
BER and Jitter Plot Generation

Circuit and system level co-simulation

Introduction

Presently favored by IC vendors for internal use

Explicitly implemented as co-simulation between a circuit level and system level simulator

Implicitly implemented as structural and behavioral modules in a AMS/SPICE simulation

The number of nodes in the circuit simulation generally governs simulation performance

- **For best results use IBIS or behavioral models for the analog portion of buffers**

It is critical to choose a tool with fast and accurate S-parameter simulation

Major Benefits

Can use the primary models used to design the silicon

Can include channel protocol logic e.g. training patterns in original design language e.g. RTL

Supports non-linear drivers and loads with complex random jitter sources

Disadvantages

No standard interface between the models and the simulator

- **Can an extension to the IBIS ATM proposal be used to solve this issue?**

Waiting for IEEE standardized HDL encryption

Example of circuit and system co-simulation

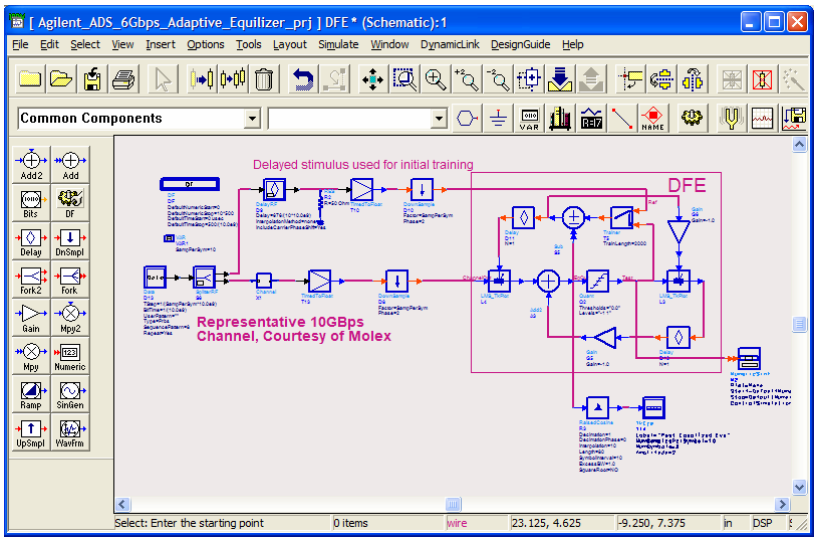
Simulation of a representative 10 Gbps channel with initial training and dynamic equalization

3000 bit training sequence

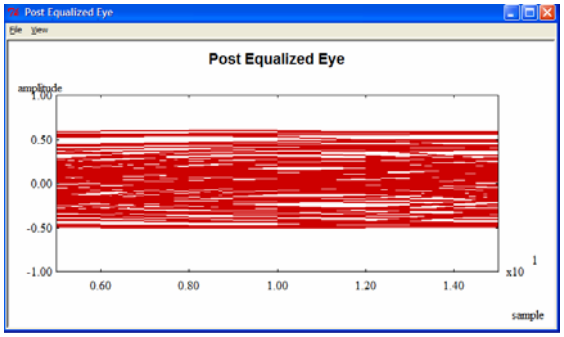
The initial eye is completely closed

The FFE and DFE coefficients can be seen to change as a function of the stimulus

Environmental variables such as supply voltage, temperature and humidity will also affect coefficients

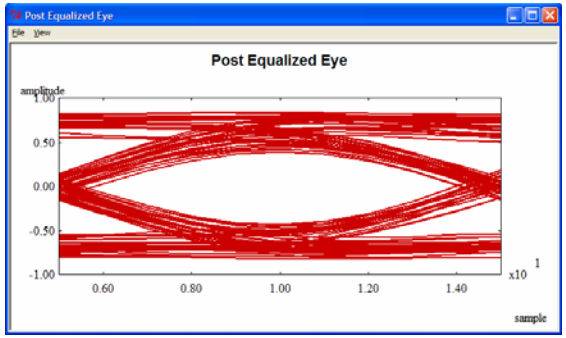


Initial Eye



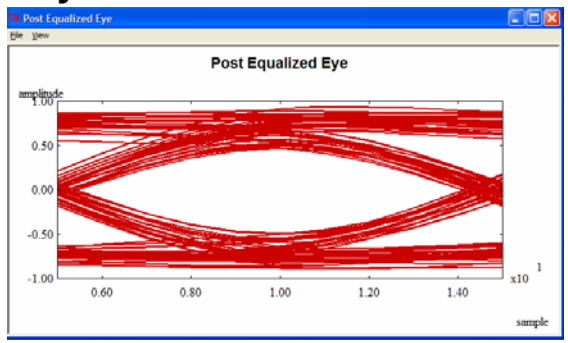
FFE and DFE coefficients

Eye after training



FFE and DFE coefficients

Eye after modified stimulus



FFE and DFE coefficients

Obtaining meaningful data from a limited dataset

Random jitter will include low probability events that have a major influence of the overall bit error rates for a channel

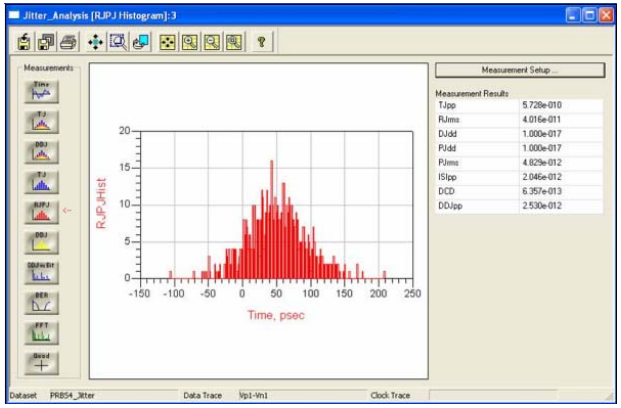
Statistical methods allow the full random jitter distribution to be predicted from the results of simulating a channel for a comparatively short number of bits

The figures on the right show the statistical separation of random jitter from the combination of deterministic jitter and random jitter and the subsequent extrapolation of a worst case BER plot

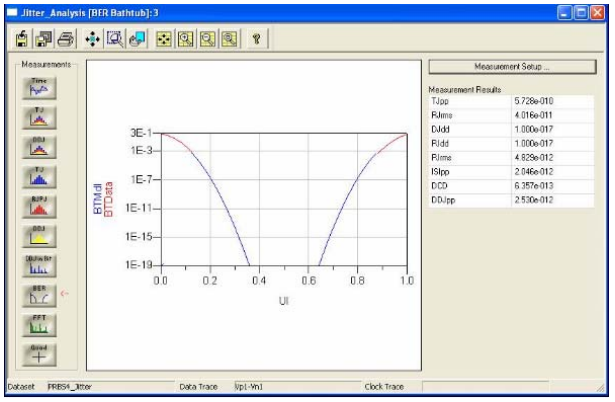
Other statistical methods such as improved importance sampling can achieve a similar result.

Instruments used to do hardware validation of multi-Gbps channels use similar statistical analysis to predict BER from a finite data sample

Jitter Analysis



Worst Case BER Plot



Observations on circuit and system co-simulation

Circuit and system co-simulation allows the behavior of multi-Gbps channels to be modeled to a very high level of accuracy

This includes the accurate modeling of random jitter and the prediction of its effect on the overall BER

It is important to note that there are many sources of random jitter

As an example, just a few sources of random jitter present in the transmitter include:

- **Thermal noise**
- **Jitter in the system clock,**
- **Jitter inherent in the clock multiplier PLL design and noise introduced into it from the reference planes**

Although this analysis of circuit and system co-simulation concentrates on driver and receiver modeling, it is also essential to also accurately model the interconnect over the full range of frequencies used for signaling.

In particular, vias and breakouts if not designed appropriately, will severely compromise channel reliability.

- **3D EM modeling is generally required**
- **Decomposition techniques that ignore the significant fringing fields generally produce inadequate results**

Established system level multi-Gbps solutions: StatEye

The StatEye tool was developed during the creation of the Optical Internetworking Forum CEI standard

Original authors: Anthony Sanders and Edoardo Prete of Infineon

Available as open source

Included as an integral part of compliance testing for multiple high speed channel standards

Provides a fast standardized analysis including:

Transmitter FFE and receiver FFE and DFE equalization with automatic optimization

Channel ISI and crosstalk noise from adjacent channels

Random jitter

Computes output pulse spectrum, bathtub curve and eye diagrams for different BER's

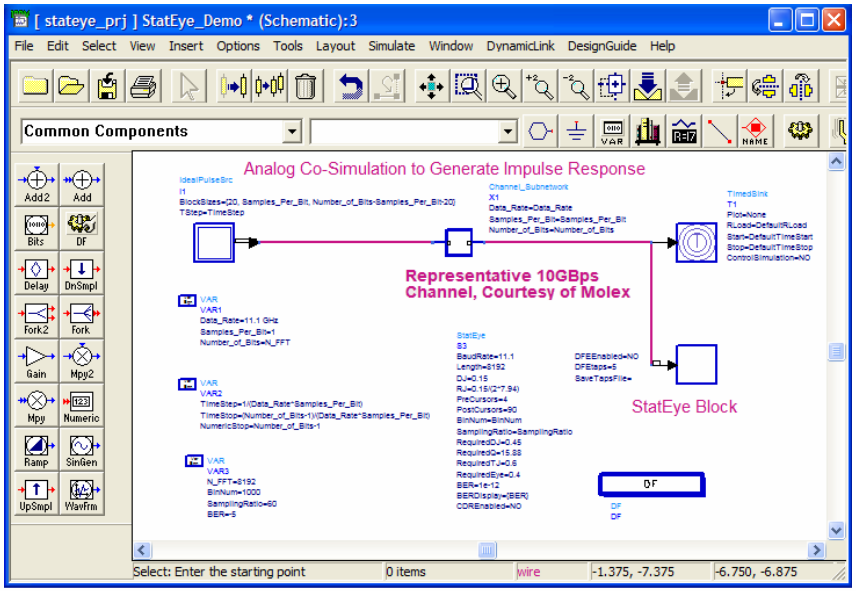
StatEye Example

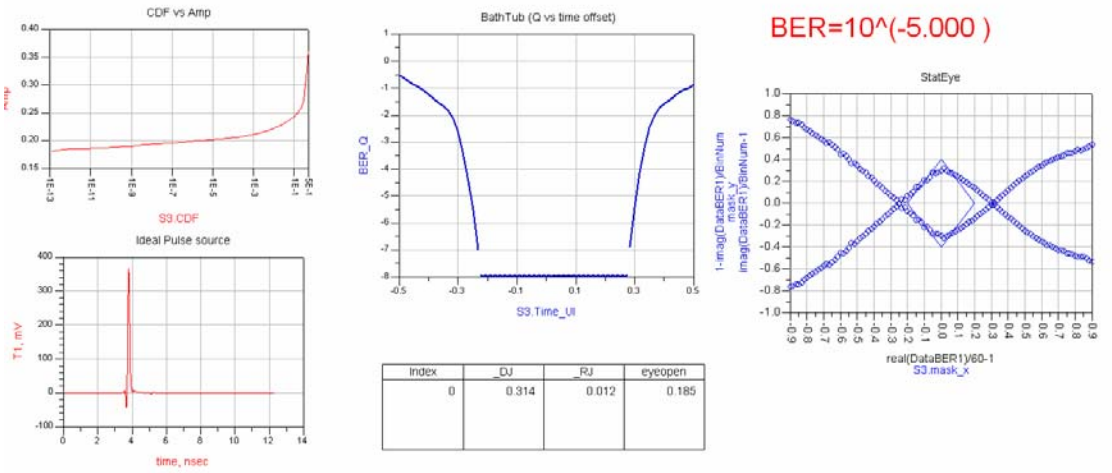
Simulation of a representative 10 Gbps channel

Circuit simulation provides the impulse response of the channel, optionally including crosstalk from adjacent channels

The StatEye module calculates the optimal FFE and DFE coefficients

The BER and statistical eye is then generated





New system level multi-Gbps solutions: IBIS ATM

There is a critical need for standardized system level analysis for multi-Gbps channels

Moving forward, we need the ability to model much more complex drivers and receivers than those presently built into StatEye.

Need transmitter and receiver models that are interchangeable between IC vendors as EDA tools

Require a standard interface so models can be automatically incorporated into simulations

The IBIS Advanced Technology Modeling working group has proposed a system level simulation framework

Well defined programmatic interfaces to algorithmic transmitter and receiver models

Standardized parameter passing

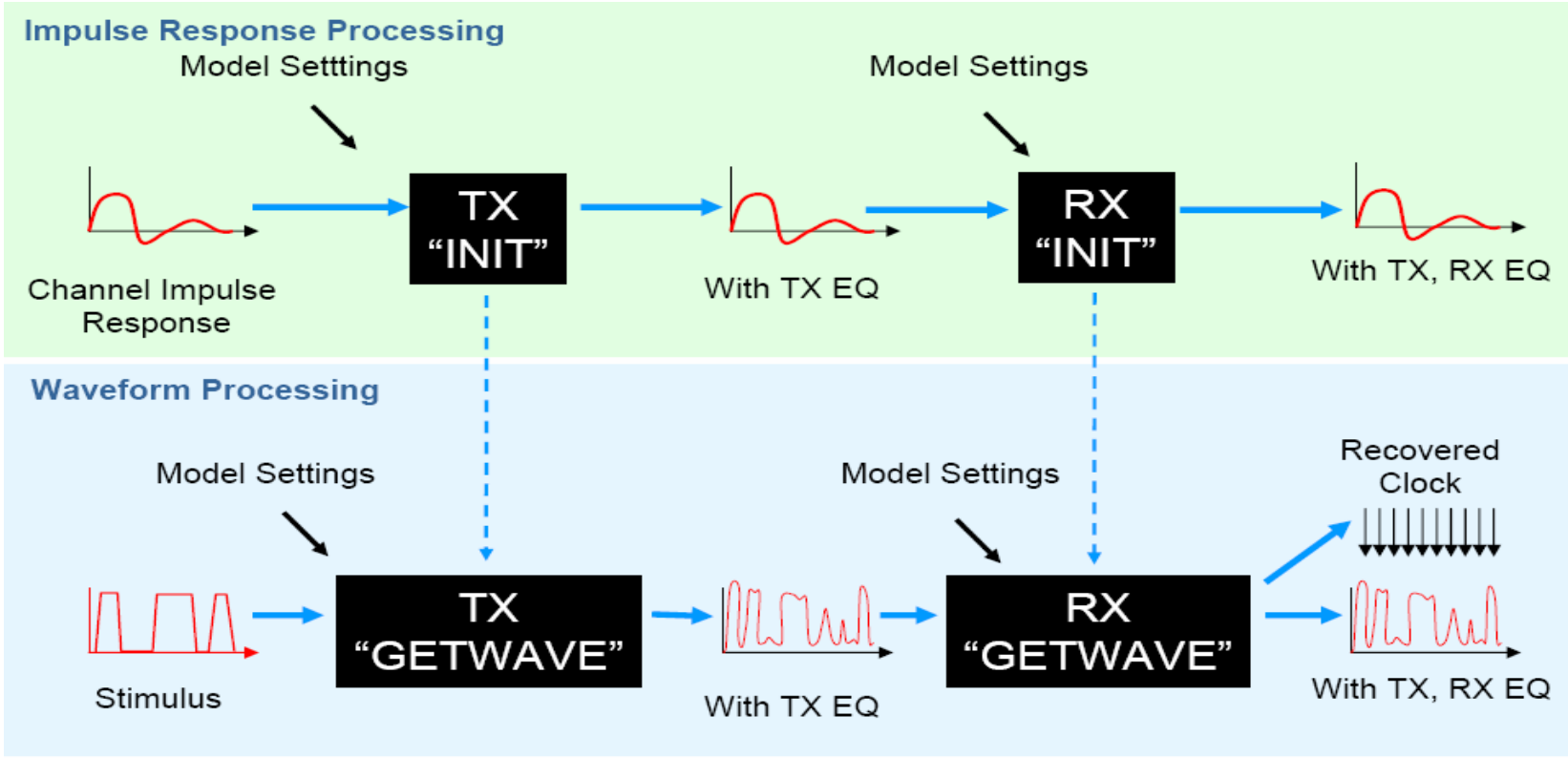
Initial effort has been to develop fast system level solutions suitable for PCB interactive and batch analysis

This framework and standardized model interface promises to solve many of the current system level simulation issues

At this time, reference models are available and their use in simulations demonstrated

Further details of the progress of the working group will be presented in an separate paper

The Standardized Interfaces of the IBIS ATM Algorithmic Transmitter and Receiver Models



Graphic courtesy of Todd Westerhoff, SiSoft

Observations on the IBIS ATM multi-Gbps proposal

The IBIS ATM working group proposal offers a flexible solution to system level multi-Gbps modeling

The working group has exhaustively considered alternate approaches and found this to be the most practical

At this time the proposal includes a well defined interface between the simulation framework and the models including parameter passing from the IBIS source file

It took a lot of hard work on behalf of the working group to achieve this result!

A general review of multi-Gbps analysis methods suggests that once the existing proposal is passed it could be further refined:

Standardized information as to which sources of jitter are included in the model

- **Allows appropriate statistical post-processing to obtain worst case BER**

A standardized approach for including RTL and other system level descriptions into the receiver and transmitter modules

- **Many IC vendors use RTL to synthesize their silicon designs**
- **The conversion of RTL into 'C' or other conventional programming languages would add costs and be a major source of modeling errors**
- **There appear to be few technical obstacles to this extension**

Conclusion

There are a multitude of approaches to multi-Gbps channel analysis

This paper has presented just a few examples

IC vendors have historically favored a combination of circuit and system level simulation

PCB system designers have a need to do system level channel analysis

The lack of a standard way of deriving system level models that protect IP from the IC vendors internal models is a major issue.

The IBIS ATM working group has made considerable progress in solving this crucial issue