Power Delivery System Design Automation

A Proposal for Specification of System-Level Design Requirements

Asian IBIS Summit, Beijing China, September 11, 2007
Agenda

- **PDS affects I/O performance**
- Technology trends
- Time domain analysis
  - SSN simulation with IBIS
- Frequency domain analysis
  - PDS impedance approach
- Recent PDS design automation
- Target Impedance in IBIS
- PDS Design Flow

Why is good PDS design important?
PDS Affects I/O Performance

- Noise from bad PDS affects *signal quality*
- Noise from bad PDS affects *timing*
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Why is PDS design more important today?
with process size shrinking, system voltages dropping, load currents rising, and clock rates increasing, good PDS design is now crucial to system performance.
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- Technology trends
- *Time domain analysis*
  - *SSN simulation with IBIS*
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- PDS Design Flow
IBIS provides effective ways to study how PDS interacts with signals in time domain
- direct indication on Peak-to-Peak noise; easily know final signal waveform with real power supply models
- rely on pattern assumptions, one simulation for one input vector

Good way to validate the final performance of system
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Frequency domain is efficient, but what impedance to specify?
Higher PDS performance corresponds to lower input impedance seen from the component (chip) into the system.

PDS impedance at the chip, looking into the package or board, can be simulated accurately with EDA tools, including the effects of: VRM, board, package, and decaps.

PDS design success can be judged by comparison of impedance to a “target” or “reference” impedance ($Z_{\text{target}}$).
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Automated PDS Design Flow
- Performance and Cost Optimization

- **Input for PDS design**
  - Physical: stack-up, layout, decap library
  - Electrical: initial decap placement or $Z_{\text{target}}$

- **Analysis and Optimization tasks for PDS**
  - Frequency domain, full-wave PDS analysis
  - Optimization of decap placement/selection

- **Results of automated EDA design flow**
  - Lowest manufacturing cost for specified system-level performance
  - Highest performance for a range of cost
  - Reduced design area
  - Interactive cost-performance tradeoffs
Nine component impedances control the optimization process.

Green curve is user-specified $Z_{\text{target}}$.

- original design used as a reference.
Optimum Performance vs. Cost

- Cost reduced by half, while maintaining the required system-level performance.
- Component-level performance details are shown.
Case 2

- Eleven component impedances control the optimization process
- No $Z_{\text{target}}$ was provided by component manufacturer
- Original design impedance used as a reference
- Interactive cost-performance tradeoffs are examined
Capacitor Configurations

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Cost: $2.67       Cost: $3.32       Cost: $5.49

- Interactive cost-performance tradeoffs quickly determine designs with both better performance and lower cost.
Case 3 - Time Domain Verification

- Frequency-domain optimization was performed first.
- All devices driven simultaneously with Gaussian current pulses.
- Time domain voltage noise performance provides an alternative mean of verifying the frequency-domain impedance performance prediction.

![Graph showing voltage over time for different designs]

- **Red**: Original design ($24.65)
- **Green**: Optimum design A ($14.04)
- **Blue**: Optimum Design B ($14.78)
- **Tan**: Optimum Design C ($16.60)
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Where to get $Z_{\text{target}}$ to define PDS design goals?
Target Impedance

- **$Z_{\text{target}}$ from simple calculation**
  - more detailed and accurate simulations are usually available

- **$Z_{\text{target}}$ from reference design** (*chip manufacturer*)
  - I/O design has applied and can generate $Z_{\text{target}}$ requirements
  - Available EDA tools are able to extract $Z_{\text{target}}$ of reference and demo designs

- **$Z_{\text{target}}$ from previous successful design** (*system manufacturer*)
  - Meet or beat actual PDS impedance of previous generation system

\[ Z_{\text{target}} = \frac{V_{dd} \times 0.05}{I \times 50\%} \]
Proposal for \( Z_{\text{target}} \) Specification in IBIS

A win-win-win scenario:
- System designers require \( Z_{\text{target}} \) to define PDS design goals.
- Chip manufacturer’s existing component-specific PI knowledge can be leveraged in a standard manner.
- EDA vendors can provide support of \( Z_{\text{target}} \) specification in IBIS to enable automated and successful PDS design.
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PDS Design Flow

- **Z\_target** profile definition should be added to IBIS.
  - leverages existing knowledge of chip vendors.
  - enables system design goals to be defined.

- EDA vendors will quickly apply this information with PDS analysis and optimization tools.

- Verification with IBIS in time domain is suggested, applying actual current profiles.

**Diagram:**

1. Determine **Z\_target** (IBIS specification or reference design)
2. Frequency domain analysis and optimization.
3. Time domain verification with IBIS
4. Successful Design
Thank You!

Advanced Power and Signal Integrity Solutions for Chips, Packages and Boards