IBIS AMI Model Developers Toolbox

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Interoperability with < 6Gbps SERDES devices

- PCB Design & Simulation env from EDA companies
  - Simulators need models
  - Models come from IC Companies
- Design Environment managed by EDA companies
- End users happy with Interoperability
Interoperability with > 6Gbps SERDES devices

- SERDES Devices that operate at 6+ Gbps can’t be modeled with current modeling standards in PCB SI space
  - FFE/DFE tap coefficient optimization
  - CDR algorithms
  - proprietary noise cancellation techniques and post-processing of data

- IC companies
  1. Forced to develop, distribute and support internal tools to model SERDES IP / IO
  2. Must protect IP

- Systems Companies
  3. Have to learn different tools from different IC companies
  4. Want interoperability
Algorithmic Modeling
Proposed Architecture & Flow

• Operate on “traditional” CA waveform output with additional algorithms
  – SERDES transmitter, receiver models as DLL
• Provide framework for customers to evaluate IP in PCB system environment that offers interoperability with other drivers/receivers
Integration with PCB Design Environment

Channel (Pkg + conn + PCBs + Backplane)

Tx + Rx

channel

Xtalk channel

Xtalk channel

Tx + Rx + Channel =

yecto
cadence
Simple API

- **Init**
  - Initialize and optimize channel with Tx / Rx Model
  - This is where the IC DSP decides how to drive the system: e.g., filter coefficients, channel compensation, …
  - Input: Channel Characterization, system and dll specific parameters from config file
    - bit period, sampling intervals, # of forward/backward coefficients, …
  - Output: Modified Channel Characterization, status

- **GetWave**
  - Modify continuous time domain waveform [CDR, Post Processing]
  - Input: Voltage at Rx input at specific times
  - Output: Modified Voltage, Clock tics, status

- **Close**
  - Clean up, exit

Parameters passed by the system simulation platform are in red
AMI_init

EDA Platform

Pass characterization

DSP algorithms modify characterization

Modified characterization

Internal storage

Model
What’s in it

• Sample Model Rx
  – Source code
  – Executable on Linux
  – Model params file

• Tester Program
  – Executable on Linux
  – Tester config file

• Starter model templates

• Documentation

• Use sample model and tester program to understand the details of the IBIS AMI API

• Create your own algorithmic models using starter model templates

• Use the tester program to test the model
Sample Rx Model

- Continuous Time Filter (CTF) RX model
  - Combination of feed forward and feed backward filter
  - Modifies the waveform given a set of coefficients
  - Tested for 6.25Gbps data rate
  - User configurable forward and backward taps

- Parameters needed by the model
  - Number of forward taps, Number of backward taps, Coefficients
  - Can be provided in a file

- To Compile:
  a) gcc -c ibis_ctf_rx.c
  b) gcc -shared -o ibis_ctf_rx.dll ibis_ctf_rx.o
CDNS AMI Tester Program

• Inputs
  – Bit Stream: “(0111100001111)”
    • Alternatively, users can specify the number of bits and let tester generate random bits
  – Data Rate
  – Impulse Response
  – DLL to interface to
  – Model specific parameters

• Outputs
  – Wave_out: *voltage-time pairs in txt file*
    waveform data modified by the Model
  – Wave_in: *voltage-time pairs in txt file*
    Represents waveform passed to the model
  – ImpulseResponse: IR data if it is modified by the model (init)
CDNS AMI Tester Program

- Usage:
  CDNS_TESTER [-h] ctf_rx_model

AMI File contains:
- Measurement Delay
- Ignore data for spec delay
- Model specific parameters

Tester config file contains:
- Information generally set by end users through the EDA platform
  - Data Rate
  - Number of bits
  - Input file names
  - Output files names
How to get the kit

- Cadence AMI Developers toolbox will be available through IBIS web site soon

- In the mean time, you can send request for the toolbox to: shah@cadence.com
Resources

• Many presentations on Algorithmic Modeling starting from June 2006 can be found at:
  http://www.vhdl.org/pub/ibis/macromodel_wip/archive-date.html

• Updates on the AMI work can also be found in ATM subcommittee updates provided at DAC 2007 and DesignCon 2007 IBIS Summits
  – Presentations can be accessed from this page:
    http://www.vhdl.org/pub/ibis/summits/

• To reach the IBIS-ATM group on this topic, you can send email to: ibis-ami-toolkit@freelists.org