IBIS-ATM Update: SerDes Modeling and IBIS

(Originally presented at the Sept 11th Summit in Beijing)
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Typical SerDes Analysis Flow

- Network Characterization
- Communication Analysis
- Analysis
- TX EQ
- RX EQ
- With TX, RX EQ
Why Two Analysis Steps?

• Performance
  – Communications analysis processes ~ 1,000,000 bits per minute
  – SPICE-based analysis throughput is much less

• Leverage existing tools and techniques
  – Communications methods & algorithms established in other domains
  – Equalization and clock recovery well suited to algorithmic description
  – Modeling/analysis algorithms are suitable for commercial numerical computation tools
Network Characterization

- Uses circuit analysis techniques to determine network behavior under reference conditions
- Characterization can take multiple forms
  - Impulse / step / pulse response (time-domain)
  - Transfer function (frequency-domain)
Communications Analysis

- Uses circuit characterization data to predict link behavior
- Many methods exist – fundamental concepts are similar, but implementation details vary
  - Commercial numerical computation tools
  - Collaboration efforts (StatEye)
  - In-house SerDes vendor solutions
  - Commercial systems-level analysis tools
SerDes Analysis

• Serial Links present new analysis requirements
  – Model SerDes TX/RX equalization
  – Model RX clock recovery behavior
  – Predict link behavior over $>> 10^7$ bits
  – Predict link bit error rate
  – Protect SerDes vendor IP

• Serial Link analysis often combines analytical methods
  – Circuit analysis (network characterization)
  – Communications analysis (equalization, clock recovery modeling)

• Modeling standards are essential, there can be no interoperable models or analysis tools without them
IBIS-ATM SerDes Task Group

• Goal: SerDes Rx/TX model interoperability
  – Multiple EDA platforms
  – Multiple SerDes vendor models
  – Protect SerDes vendor IP
• IBIS-ATM committee participation
  – EDA: Agilent, Cadence, Mentor, SiSoft
  – Semiconductor: IBM, Intel, Micron, ST-Micro, TI, Xilinx
  – System: Cisco
• Two part modeling standard
  – Characterization model: existing IBIS syntax models TX / RX analog characteristics
  – Algorithmic model: equalization, clock recovery, device optimization algorithms
IBIS-AMI Serial Link Analysis

TX

- Serializer
- Transmit Equalizer
- Package Interconnect
- System Interconnect
- Package Interconnect

RX

- Receive Equalizer
- Clock Recovery
- Data Recovery

TX EQ
LTI or non-LTI

- TX Equalization
- TX Optimization

Channel & Analog I/O
Linear, Time-Invariant

- Channel Characterization (Impulse response)

RX EQ, CDR
LTI or non-LTI

- RX Equalization
- RX Clock Recovery
- RX Optimization
IBIS-ATM Algorithmic Models

• Communication models provided as [binary] code
  – Fast, efficient execution
  – Protects vendor IP
  – Extensible modeling capability
  – Allows models to be developed in multiple languages

• Standardized execution interface
  – Module loading mechanism & call signature
  – Data input/output formats

• Standardized model parameter interface
  – “Reserved parameters” interpreted by EDA platforms
  – Model-specific parameters can be exposed to and set by end-users
IBIS-ATM Algorithmic Models

**Impulse Response Processing**
- Model Settings

  ![Channel Impulse Response](image)

  ![Model Settings](image)

  ![TX "INIT"](image)

  ![With TX EQ](image)

  ![RX "INIT"](image)

  ![With TX, RX EQ](image)

**Waveform Processing**
- Model Settings

  ![Stimulus](image)

  ![Model Settings](image)

  ![TX "GETWAVE"](image)

  ![With TX EQ](image)

  ![RX "GETWAVE"](image)

  ![With TX, RX EQ](image)

  ![Recovered Clock](image)

  ![With TX, RX EQ](image)
Executable (DLL) Call Arguments

- **Init** (impulse response processing)
  - Bit time
  - Number of waveform samples per bit
  - Number of crosstalk aggressors
  - Channel impulse response(s)
  - Model parameters and values
  - Pointers to free memory, data return area

- **Getwave** (waveform processing)
  - Input waveform(s)
  - Pointers to data return area
    - Equalized waveform
    - Clock times
    - Optimized parameters
Model Parameters

Additional data passed between executable model & simulator:

• Model-specific parameters
  – Allow IP vendors to define data required for / provided by a specific model
  – Defined parameter declaration and usage format
    • Allows end-users to set and display model-specific data

• Reserved parameters
  – Predefined parameter list used by EDA tools to alter analysis flow
  – Allows models to tell EDA platform what data the model does/doesn’t provide
IBIS-ATM Status

• Original proposal submitted by Cadence & IBM
  – Current version authored by Cadence, Mentor, SiSoft

• First draft of BIRD approved by IBIS-ATM task group for prototype model & EDA platform development
  – Prove interoperability & refine proposal before bringing back to IBIS Open Forum

• Subcommittee work, presentations & BIRD available on-line:
  – http://www.vhdl.org/pub/ibis/macromodel_wip/

• Public TX/RX models, modeling “toolkits” will be available
## Next Steps

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<th>Preliminary approval by IBIS-ATM subcommittee</th>
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<tr>
<td>√</td>
<td>Complete BIRD documentation</td>
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<td>Develop sample models &amp; prototype EDA integration; demonstrate interoperability</td>
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**Target:**

- **Sep 2007**: Refine BIRD based on prototype experience
- **Oct 2007**: Bring to IBIS-ATM task group for final approval
- Bring BIRD to IBIS Open Forum for approval
- Incorporate BIRD into updated IBIS specification