Power Delivery System Design Automation

A Proposal for Specification of System-Level Design Requirements

Asian IBIS Summit, Tokyo, Japan
September 14, 2007

Originally presented at the Sept. 11 Summit in Beijing, China
Agenda

- **PDS affects I/O performance**
- Technology trends
- Time domain analysis
  - SSN simulation with IBIS
- Frequency domain analysis
  - PDS impedance approach
- Recent PDS design automation
- Target Impedance in IBIS
- PDS Design Flow
PDS Affects I/O Performance

- Noise from bad PDS affects *signal quality*

- Noise from bad PDS affects *timing*
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With process size shrinking, system voltages dropping, load currents rising, and clock rates increasing, good PDS design is now crucial to proper system performance.
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IBIS enables time domain PDS performance verification
IBIS provides an effective means to study how the PDS and signals interact
- Direct indication of Peak-to-Peak noise
- Produces signal waveforms with real power supply and return currents
- Relies on pattern assumptions, one simulation for one input vector

Common methodology to validate final performance of system
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- **Frequency domain analysis**
  - *PDS impedance approach*
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Higher PDS performance corresponds to lower input impedance seen from the component (chip) into the system.

PDS impedance at the chip, looking into the package and board, can be simulated accurately with EDA tools, including the effects of: VRM, board, package, and decaps.

PDS design success can be judged by comparison of actual impedance to a “target” impedance (\(Z_{\text{target}}\)).
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Automated PDS Design Flow
- Performance and Cost Optimization

- **Input for PDS design**
  - Physical: stack-up, layout, decap library
  - Electrical: initial decap placement, $Z_{\text{target}}$

- **Analysis and Optimization tasks for PDS**
  - Frequency domain, full-wave PDS analysis
  - Optimization of decap placement/selection

- **Results of automated EDA design flow**
  - Lowest manufacturing cost for specified system-level performance
  - Highest performance for a given cost target
  - Reduced design area
  - Interactive cost-performance tradeoffs
Nine component impedances control the optimization process

- Green curve is the user-specified Z_target
  - Original design used as a reference
Optimum Performance vs. Cost

- Cost reduced by half, while maintaining the required system-level performance
- Component-level performance details are shown
Case 2

- Eleven component impedances control the optimization process
- No $Z_{\text{target}}$ was provided by component manufacturer
- Original design impedance used as the target
- Interactive cost-performance tradeoffs are examined
## Capacitor Configurations

### Optimum Design A

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Cost: **$2.67**

### Optimum Design B

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Cost: **$3.32**

### Original Design

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Cost: **$5.49**

- Interactive cost-performance tradeoffs quickly determine designs with both better performance and lower cost.
Case 3 - Time Domain Verification

- Frequency-domain optimization is performed first
- All devices driven simultaneously with Gaussian current pulses
- Time domain voltage noise performance provides an alternative means of verifying the frequency-domain impedance performance prediction

![Graph showing voltage over time for different designs: Red: Original design ($24.65), Green: Optimum design A ($14.04), Blue: Optimum Design B ($14.78), Tan: Optimum Design C ($16.60)]
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Where to get Z_target to define PDS design goals?
**Target Impedance**

\[ Z_{target} = \frac{V_{dd} \times 0.05}{I \times 50\%} \]

- **\( Z_{target} \) from simple calculation**
  - more detailed and accurate simulations are usually available

- **\( Z_{target} \) from reference design (chip manufacturer)**
  - I/O cell design completed and can generate \( Z_{target} \) requirements
  - Available EDA tools are able to extract \( Z_{target} \) of reference and demo designs

- **\( Z_{target} \) from previous successful designs (system manufacturer)**
  - Meet or beat actual PDS impedance of previous generation system
Proposal for $Z_{\text{target}}$ Specification in IBIS

A win-win-win scenario:
- System designers require $Z_{\text{target}}$ to define PDS design goals.
- Chip manufacturer’s existing component-specific PI knowledge can be leveraged in a standard manner.
- EDA vendors can provide support of $Z_{\text{target}}$ specification in IBIS to enable automated and successful PDS design.
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PDS Design Flow

- **Z_{target} profile definition proposal**
  - Leverages existing knowledge of chip vendors
  - Enables system design goals to be defined

- EDA vendors can quickly apply this information with PDS analysis and optimization tools

- Verification with IBIS in time domain is suggested, applying actual current profiles.

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Determine Z_{target} (IBIS specification or reference design)

Frequency domain analysis and optimization

Time domain verification with IBIS

Successful Design
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Sigrity, Inc.

Key to the Power and Signal Integrity
Solution for IC Packages and PCBs