Interconnect Modeling Using IBIS-ISS and Touchstone

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Presented by Mike LaBonte, SiSoft

IBIS Summit at EDICON 2017
Agenda

- History
- The Need for Improved Interconnect Support
- Principles of the Interconnect Proposal
  - Structure
  - Terminals, Models and Sets
  - New Keywords
- An Example Explained
- Summary
History

- Interconnect Task Group resumed meeting in early 2014
  - Received draft BIRD from Walter Katz (SiSoft) to support IBIS-ISS packages within IBIS

- BIRD189.4 available for review
  - [http://www.ibis.org/birds/birds189.4.docx](http://www.ibis.org/birds/birds189.4.docx)
  - ~40 pages with examples
  - Comments welcome

- Intended for IBIS Version 7.0

- Brief overview with some key points is given here
Why Update Interconnect Modeling?

- Improve package models with IBIS-ISS (a Synopsys HSPICE* subset) and Touchstone support

- Package modeling in IBIS unchanged since 2000
  - [Pin], [Package], [Package Model]
  - [Alternate Package Models] selector added
  - Limited support of loss, crosstalk and/or partitioning

- EBD (Electrical Board Description) for boards: no coupling and limited package model application

- IBIS, IBIS-ISS, Touchstone 2.0 and ICM are separate specifications
  - Limited interaction between them for package modeling
  - ICM (Interconnect Model) never adopted by industry
Features of the Interconnect Proposal

- Supports…
  - IBIS-ISS and Touchstone models (common in industry)
  - Both I/O and supply (POWER and GND) connections
  - (New) optional Die pad interface between Pins and Buffers
  - I/O pin_names as terminal qualifiers
    - May have optional Aggressor_Only designation
  - POWER and GND terminal qualifiers by pin_name, pad_name, signal_name or [Pin Mapping] bus_label for rail connections with direct or combined terminals
  - Plus many other features not covered here…

A few objectives for the Interconnect Modeling proposal
**Structure of the Interconnect Proposal**

Introduces optional Die Pad interface for terminals separate from Buffer and Pin terminals

- **NEW!**
  - pin_names, signal_names, and model_names from the [Pin] keyword

[Model] buffer definition but with explicitly identified terminals
Relates to Physical Structures

One-to-one path connection; Die Pad interface optional; Aggressor_Only designation optional.

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Terminals at Buffer, Die Pad and Pin Interfaces

Original IBIS (4.0 and earlier)
- Pins are explicit
- Buffer terminals implicit in [Model]
- Die pad terminals same as buffer terminals
- Packages defined connections between pins and buffers

Current Proposal
- Die pad terminals are now explicit
- Buffer terminals are now explicit
- [Pin]s are… still pins
- Separate interconnect definitions can be created between …
  - Pin-to-Die pad terminals,
  - Die pad-to-Buffer terminals,
  - Pin-to-Buffer terminals (still) supported
Physical Rails (Can be Merged)
New Keywords and Subparameters
(Limited Discussion Here)

- [Bus Labels] | bus_label
- [Die Supply Pads] | pad_name, optional bus_label
- [Interconnect Model]/[End Interconnect Model]
  - Param | parameter passing
  - File_IBIS-ISS | names IBIS-ISS file
  - File_TS | names Tstone file
  - Number_of_terminals=<value> | number of terminals
  - <terminal lines> | described later
- [Interconnect Model Set]/[End Interconnect Model Set]
- [Interconnect Model Set Selector]/[End Interconnect Model Set Selector]
Interconnect Models

- Connections between terminals with IBIS-ISS or Touchstone files
- Terminal connection points at Buffer, Die pad, or Pin interfaces
- Identifies rail or I/O terminals
- Allows pin_name, signal_name, pad_name, or bus_label terminal qualifiers for rails (and pin_name for I/O terminals)
- Identifies whether a coupled signal is only an aggressor or also “experiences” coupling from other sources

How package and on-die electrical information is generated and delivered today
[Interconnect Model Set]s

- Groups Interconnect Models
- Can be used (and is recommended) to establish a complete path
- Can be grouped with selection controls for individual simulations, similar to [Model] and [Model Selector]

Some Example Groupings and Applications
- Separate sets, one per interface (e.g., memory, network)
- Separate sets for coupled vs. single-line simulations
- Different sets for different power delivery network complexities
  - POWER connected at single pin, single buffer terminal
  - POWER connected through multiple pins, rails to individual buffer terminals
<Terminal lines> Syntax

- All column entries on one line:

  `<Terminal_number>` `<Terminal_type>`
  `<Terminal_type_qualifier>` `<Qualifier_entry>`
  `[Aggressor_Only]

- `<Terminal_number>` is **IBIS-ISS node position** or **Touchstone port number**

- Allowable `<Terminal_type>` names and associations next
**Allowable `<Terminal_type>` Associations**

<`Terminal_number>` `<Terminal_type>` `<Terminal_type_qualifier>` `<Qualifier_entry>` [Aggressor_Only]

<table>
<thead>
<tr>
<th>Terminal_type</th>
<th>Terminal_type_qualifier</th>
<th>Aggressor_Only</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>pin_name</td>
<td>signal_name</td>
</tr>
<tr>
<td>Pin_I/O</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Pad_I/O</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Buffer_I/O</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Pin_Rail</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>Pad_Rail</td>
<td></td>
<td>Y</td>
</tr>
<tr>
<td>Buffer_Rail</td>
<td></td>
<td>Y</td>
</tr>
<tr>
<td>Pullup_ref</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Pulldown_ref</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Power_clamp_ref</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Gnd_clamp_ref</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Ext_ref</td>
<td>X</td>
<td></td>
</tr>
</tbody>
</table>

<Qualifier_entry>: ”X” I/O pin_name; “Y,” or “Z”: POWER or GND name. Optional “A”: “Aggressor_Only”
Example Showing Connections

Buffer Terminals  Die Pad Terminals  Pins

C1 VDD  POWER
A1 DQ1  DATA_MODEL
C2 VSS  GND
A2 DQ2  DATA_MODEL

VDDQ
VSSQ
The [Die Supply Pads] keyword establishes pad_name <Qualifier_entries> for rails, and associates them with signal_name (and optionally with bus_label entries).

```
[Die Supply Pads] signal_name bus_label
| pad_name
  VDDQ    VDD
  VSSQ    VSS
```
[Interconnect Model] for Buffer-to-Die Pad Side

[Interconnect Model Set] Full_ISS_PDN
| [Interconnect Model] Partial_ISS_buf_pad
| File_IBIS-ISS buf_pad.iss buf_pad_2_typ
Number_of_terminals = 10
| 1 Pad_I/O pin_name A1 | DQ1 (DQ signal)
  2 Pad_I/O pin_name A2 | DQ2 (DQ signal)
  3 Pullup_ref pin_name A1 | VDD (POWER connection)
  4 Pulldown_ref pin_name A1 | VSS (GND connection)
  5 Buffer_I/O pin_name A1 | DQ1 (DQ signal)
  6 Pullup_ref pin_name A2 | VDD (POWER connection)
  7 Pulldown_ref pin_name A2 | VSS (GND connection)
  8 Buffer_I/O pin_name A2 | DQ2 (DQ signal)
|  9 Pad_Rail pad_name VDDQ | VDD POWER
  10 Pad_Rail pad_name VSSQ | VSS GND
| [End Interconnect Model]
[Interconnect Model] for
Buffer-to-Die Pad Side (Expanded)

[Interconnect Model Set] Full_ISS_PDN
|
[Interconnect Model] Partial_ISS_buf_pad
|
File_IBIS-ISS   buf_pad.iss   buf_pad_2_typ
Number_of_terminals = 10
|
1  Pad_I/O     pin_name     A1 | DQ1 (DQ signal)
2  Pad_I/O     pin_name     A2 | DQ2 (DQ signal)
|
| POWER and GND terminals with pad_names and pin_names
3  Pullup_ref  pin_name     A1 | VDD (POWER connection)
4  Pulldown_ref pin_name    A1 | VSS (GND connection)
5  Buffer_I/O   pin_name    A1 | DQ1 (DQ signal)
6  Pullup_ref  pin_name     A2 | VDD (POWER connection)
7  Pulldown_ref pin_name    A2 | VSS (GND connection)
8  Buffer_I/O   pin_name    A2 | DQ2 (DQ signal)
|
| POWER and GND terminals with signal_names
9  Pad_Rail     pad_name    VDDQ | VDD  POWER
10 Pad_Rail     pad_name    VSSQ | VSS  GND
|
[End Interconnect Model]
[Interconnect Model] for Die Pad-to-Pin Side

Buffer Terminals

Die Pad Terminals

Pins

C1 VDD POWER
A1 DQ1 DATA_MODEL
C2 VSS GND

A2 DQ2 DATA_MODEL

[Interconnect Model] Partial_ISS_pad_pin_2

File_IBIS-ISS pad_pin.iss pad_pin_2_typ
Number_of_terminals = 8

1 Pin_I/O pin_name A1 | DQ1 (DQ signal)
2 Pin_I/O pin_name A2 | DQ2 (DQ signal)

POWER and GND terminals with signal_names
3 Pin_Rail signal_name VDD | VDD (POWER connection)
4 Pin_Rail signal_name VSS | VSS (GND connection)

POWER and GND terminals with pad_names
5 Pad_I/O pin_name A1 | DQ1 (DQ signal)
6 Pad_I/O pin_name A2 | DQ2 (DQ signal)

[End Interconnect Model]

[End Interconnect Model Set]
[Interconnect Model] for Die Pad-to-Pin Side (Expanded)

File and subcircuit

[Interconnect Model] Partial_ISS_pad_pin_2

File_IBIS-ISS  pad_pin.iss  pad_pin_2_typ

Number of terminals = 8

1  Pin_I/O  pin_name  A1  |  DQ1 (DQ signal)
2  Pin_I/O  pin_name  A2  |  DQ2 (DQ signal)

POWER and GND terminals with signal_names
3  Pin_Rail  signal_name  VDD  |  VDD (POWER connection)
4  Pin_Rail  signal_name  VSS  |  VSS (GND connection)

POWER and GND terminals with pad_names
5  Pad_I/O  pin_name  A1  |  DQ1 (DQ signal)
6  Pad_I/O  pin_name  A2  |  DQ2 (DQ signal)

POWER and GND terminals with pad_names
7  Pad_Rail  pad_name  VDDQ  |  pad_name with VDD
8  Pad_Rail  pad_name  VSSQ  |  pad_name with VSS

[End Interconnect Model]

[End Interconnect Model Set]
Complete [Interconnect Model Set] With Both [Interconnect Model]s

[Interconnect Model Set] Full_ISS_PDN

[Interconnect Model] Partial_ISS_buf_pad

File_IBIS-ISS  buf_pad.iss  buf_pad_2_typ

Number_of_terminals = 10

1  Pad_I/O  pin_name  A1  |  DQ1 (DQ signal)
2  Pad_I/O  pin_name  A2  |  DQ2 (DQ signal)

| POWER and GND terminals with pad_names and pin_names
3  Pullup_ref  pin_name  A1  |  VDD (POWER connection)
4  Pulldown_ref  pin_name  A1  |  VSS (GND connection)
5  Buffer_I/O  pin_name  A1  |  DQ1 (DQ signal)
6  Pullup_ref  pin_name  A2  |  VDD (POWER connection)
7  Pulldown_ref  pin_name  A2  |  VSS (GND connection)
8  Buffer_I/O  pin_name  A2  |  DQ2 (DQ signal)

| POWER and GND terminals with signal_names
9  Pad_Rail  signal_name  VDDQ  |  VDD POWER
10 Pad_Rail  signal_name  VSSQ  |  VSS GND

[End Interconnect Model] Partial_ISS_pad_pin_2

File_IBIS-ISS  pad_pin.iss  pad_pin_2_typ

Number_of_terminals = 8

1  Pin_I/O  pin_name  A1  |  DQ1 (DQ signal)
2  Pin_I/O  pin_name  A2  |  DQ2 (DQ signal)

| POWER and GND terminals with signal_names
3  Pin_Rail  signal_name  VDD  |  VDD (POWER connection)
4  Pin_Rail  signal_name  VSS  |  VSS (GND connection)
5  Pad_I/O  pin_name  A1  |  DQ1 (DQ signal)
6  Pad_I/O  pin_name  A2  |  DQ2 (DQ signal)

| POWER and GND terminals with pad_names
7  Pad_Rail  pad_name  VDDQ  |  VDD is signal name
8  Pad_Rail  pad_name  VSSQ  |  VSS is signal name

[End Interconnect Model]
Summary

- BIRD189.4 improves IBIS package modeling
  - More revisions coming through the IBIS Interconnect Task Group

- Links IBIS, IBIS-ISS and Touchstone for package models
  - Adds flexible support for package loss, crosstalk and partitioning

- Formalizes and separates Die pads and Buffers

- Other extensions (not covered here) included

New advanced Interconnect format for IBIS Version 7.0!