Leveraging IBIS Capabilities for Multi-Gigabit Interfaces

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Overview

- In writing EDI CON paper “Signal Integrity Methodology for Double-Digit Multi-Gigabit Interfaces”, different IBIS modeling techniques were applied
- Wanted to share some of the IBIS modeling methods we’ve been using
Agenda

• [External Model]
• AMI equalization adaptation
• Backchannel training
• Applying IBIS-AMI to DDR applications
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Preliminary IBIS Modeling

- Can get started with:
  - Voltage swing
  - Pad capacitance
  - Output impedance
  - Rise time

- Even easier to model using [External Model] syntax

```plaintext
[Model] pcell_out
Model_type Output
Polarity Non-Inverting
Vnms = 0.5

<table>
<thead>
<tr>
<th>variable</th>
<th>typ</th>
<th>min</th>
<th>max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ccomp</td>
<td>0.50pF</td>
<td>0.50pF</td>
<td>0.50pF</td>
</tr>
</tbody>
</table>

[Temperature Range]

<table>
<thead>
<tr>
<th>Voltage</th>
<th>I(typ)</th>
<th>I(min)</th>
<th>I(max)</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>-2.0e-02</td>
<td>-2.0e-02</td>
<td>-2.0e-02</td>
</tr>
<tr>
<td>80</td>
<td>0.0e-00</td>
<td>0.0e-00</td>
<td>0.0e-00</td>
</tr>
<tr>
<td>-50</td>
<td>2.0e-02</td>
<td>2.0e-02</td>
<td>2.0e-02</td>
</tr>
</tbody>
</table>

[Temperature Range]

<table>
<thead>
<tr>
<th>Voltage</th>
<th>I(typ)</th>
<th>I(min)</th>
<th>I(max)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>0.0</td>
<td>0.0</td>
<td>0.0</td>
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<tr>
<td>1.0</td>
<td>2.0e-02</td>
<td>2.0e-02</td>
<td>2.0e-02</td>
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<tr>
<td>1.0</td>
<td>2.0e-02</td>
<td>2.0e-02</td>
<td>2.0e-02</td>
</tr>
</tbody>
</table>

[Ramp]

<table>
<thead>
<tr>
<th>variable</th>
<th>typ</th>
<th>min</th>
<th>max</th>
</tr>
</thead>
<tbody>
<tr>
<td>dV/dt_c</td>
<td>0.0</td>
<td>0.020n</td>
<td>0.020n</td>
</tr>
<tr>
<td>dV/dt_f</td>
<td>0.0</td>
<td>0.020n</td>
<td>0.020n</td>
</tr>
</tbody>
</table>

R_load = 50
```
External Model

• Originally introduced in IBIS 4.1!
• Enabled VHDL, Verilog-A, and Spice syntax to be used for buffer models instead of VI/VT table syntax
• Spice syntax has proven very useful to us
Spice [External Model]s Convenient for Early Feasibility

- Sometimes the IBIS model you want is not available for preliminary / pre-design analysis.
- Easy to write (or use) simple parameterized Spice subcircuits for IO buffers when IBIS availability does not align with your project schedule.
- Can sweep parameters and cover a big portion of the design space quickly and easily.
Analog Buffer Model Extensions

• Incorporated into IBIS 6.0

```
[External Model]
Language IBIS-ISS
|
| Corner corner_name file name circuit_name (.subckt name)
Corner Typ cdns_txxrx.cir tx_subckt
|
| List of parameters
Parameters ISSfile = cdns_txx.param(CDNS_Tx(Model_Specific(Txnoise)));
Parameters Tx_Rseries = cdns_txx.param(CDNS_Tx(Model_Specific(Tx_R)));
|
| List of converter parameters
ConverterParameters Vtx_h = cdns_txx.param(CDNS_Tx(Model_Specific(Tx_V)));
|
| Ports List of port names (in same order as in SPICE)
Ports A_signal_pos A_signal_neg my_driveP A_pdef A_puref
|
| D_to_A d_port port1 port2 vlow vhigh rise fall corner_name polarity
D_to_A D_drive my_driveP A_pdef 0 Vtx_h 0.03n 0.03n Typ
|
| [End External Model]
```

Tx/Rx Model described in external file

• Replaces the VI/VT curves
• Can now be parameterized when Language ‘IBIS-ISS’ is used

Parameter Definition is in a separate file

• Similar to AMI Parameters
• Can be in .ami or any other file
• User Selects Parameter Values from GUI

Parameter Value is passed to Simulator

• Using .param, the parameter value is passed to the simulator
• Converter_Parameters are used appropriately in the stimulus/D_to_A

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Agenda

• [External Model]
• **AMI equalization adaptation**
• Backchannel training
• Applying IBIS-AMI to DDR applications
Anatomy of a Receiver AMI Model

- These different modules typically adapt at different rates
- Initial modules usually adapt more slowly than later ones

- Curve-based function to boost the incoming signal so that it could be detected at the output.
  - Noise also gets boosted.

- Selective boosting at frequency of interest (high freq channel loss cancellation)
  - Better for Area/Pwr considerations
  - Noise and xtalk also gets boosted.
  - Usually first order filter only

- Feeds back previous bit decisions to cancel post cursor ISI caused by them
  - Can model non-linearity
  - Adaptively tunes tap coeff.
  - Level sensitive
  - Cannot cancel pre-cursor
  - Needs 'something' to work with → AGC/CTLE

- AGC
- CTLE
- DFE + CDR
Rx With Default Adaptation

• Note that adaptation coefficients don’t converge
With Faster AGC Adaptation

• Coefficients converge, but after 150k bits of traffic are passed
Ignoring the First 150k Bits

- Default was to ignore the first 40k bits
- Eliminates the noise from before coefficients converged
- Very important to be able to visualize how the adaptation is converging
Original Eye Contour vs. Final

- Adjusting AGC adaptation time and Ignore_Bits made a significant difference in eye height.
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Backchannel Training (IBIS BIRD 147, in IBIS 7.0)

- Rx feeds back EQ adjustments to Tx during training
- Then data is passed with adjusted Tx settings in place
With and Without Backchannel

- Backchannel turned down Tx FFE settings somewhat
- Leaves more “heavy lifting” to Rx and its advanced adaptation
- Improves overall signal quality significantly
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DDR4 Brought Some New Requirements

• Specified DQ mask compliance checking at a particular BER
• BER analysis requires extrapolation (bathtubs)
• Extrapolation requires a lot of traffic to be passed (need a lot of samples)
  – Channel simulation can be applied
• Started to see equalization used at Controller side
  – AMI modeling can be applied
• Worked with IP division to develop AMI model for DDR4 IP
CTLE Correlation: 3200Mbps

Input of receiver @pad

Output of CTLE

IBIS-AMI channel sim

Transistor-Level circuit sim
CTLE + DFE Correlation: 3200Mbps

Transistor-Level circuit sim

IBIS-AMI channel sim
Summary

- External Model syntax can be very useful for pre-design modeling, when detailed IBIS models are not available, and has had some recent additions in capability.
- Building IBIS-AMI models is not the obstacle it used to be.
- Adaptive equalization often has interplay between multiple sub-modules in real devices, and therefore also in AMI models.
- If adaptive, understand if your EQ coefficients converge during simulation.
- Backchannel training enables interplay between the Tx and Rx in simulation, and can produce more realistic results for devices that use backchannel.
- Channel simulation and AMI modeling has been successfully applied to DDR4 IP (and more of this is expected with DDR5).