IBIS FORUM
I/O BUFFER MODELING COOKBOOK

Revision 1.0

Prepared By:

Stephen Peters

John Chehab

John Lee

Robin Rosenbaum

Intel Corporation, Hillsboro OR

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Introduction

This cookbook describes the major steps required to produce IBIS models for digital integrated circuit (IC) input, output, and I/O buffers. IBIS stands for I/O Buffer Information Specification, a way to present the electrical characteristics of an input, output, or I/O buffer behaviorally, i.e., without revealing the underlying transistor or process information. This cookbook applies to models generated for IBIS V1.1. For additional IBIS and IBIS Forum introductory information, see the *IBIS Overview*.

The information contained in this cookbook can be used to model CMOS and bipolar parts.

Descriptive information is needed about the buffers to construct an accurate behavioral model. The purpose of this document is to explain how to gather this information via either direct measurement or silicon simulation and how to format the gathered data for publication or for machine-readable use.

To behaviorally represent any such buffer requires the following information:

- the I-V characteristics of the power clamp or ESD diodes
- the input or output capacitance of the buffer
- the characteristics of the package (the values of the lead inductance, resistance, and capacitance)

Output and I/O buffer representations also require:

- the current vs. voltage (I-V) characteristics of the buffer in both low and high states
- the rise and fall time of the buffer when switching

The information gathered is collected into an ASCII file in a standard machine-readable format for simulator input and other electronic needs.

The most recent version of the specification, the latest version of the *IBIS Overview*, and other IBIS documents are available on the Internet from the machine "vhdl.org". For access information, see the *Resources* section later in this cookbook.

To create an IBIS model, do the following:

1. Perform the pre-modeling steps. These include obtaining the packaging information, determining the voltage and temperature tolerances over which the IC is specified to operate, and obtaining other information about the device. See the section titled *Pre-Modeling Steps*.
2. Obtain the I-V curves and rise/fall times for output or I/O buffers either by direct measurement or by simulation. Use the analog models and simulator supported by the IC or ASIC vendor. See the section titled *Extracting the Data*.
3. Fill out an IBIS data sheet. See the section titled *Putting the Data Into an IBIS File*.
4. If the model is generated from simulated data, validate the model by comparing the results from the original analog model using IBIS against results from the simulator used to generate the data. See the section titled *Validating the Model*.
5. From measured data, compare the IBIS model output to the measured output. See the section titled *Correlating the Data*.

Pre-modeling Steps

GATHERING INFORMATION

To perform a complete and correct simulation of your circuit, you need the following:

Schematic	You need the schematic both to determine how many unique buffer designs are on the chip and to simulate the design.
Package/voltage combinations	Find out in what packages the device is offered. A separate IBIS model is required for each package type. Also determine whether the I/O buffers are designed to operate in a mixed power supply system. ESD diodes might be referenced to a different supply than the buffer.
V_{CC} limits and signal information	Acquire a copy of the data book or equivalent information. Determine the voltage and temperature limits over which the device is designed to operate. Also determine which signals can be ignored for modeling purposes. For example, static control signals may not need an I/O model.
Packaging information	You need the signal-name-to-pin mapping information and the electrical information for each pad-to-pin connection.
Die capacitance	Finally, get the input, output, or I/O capacitance of each pad, seen when you look from the **pad** back into the buffer for a fully placed and routed buffer design.

DETERMINING HOW MANY MODELS PER IC

An IC can use one or more buffer designs. The trend is toward using fewer or a single type of output structure (size and connection of the transistor elements) to drive the chip output and I/O signals. For a single output structure, all the outputs and I/O signals have the same I-V characteristics and rise/fall times.

However, even when all outputs or I/O use the same buffer design, not all the outputs and I/O can be represented by a single I/O buffer model. Because of differences in output capacitance, signal functions (outputs vs. I/O cells), and packaging parameters, different signals can require different I/O buffer models. While grouping signals into appropriate I/O buffer models is a matter of experience, here are some general guidelines:

- Separate inputs from output and I/O signals. Input models can require I-V curves but no rise/fall time information. Input signals are differentiated by input die capacitances and packaging parameters. Group together signals with similar input die capacitances and packaging R/L/C values.
- It is generally good practice to group output and I/O signals first according to signal function, then according to output die capacitance and packaging. For example, when modeling a microprocessor segregate the address bus, data bus and control signals into three groups, then further divide them by the output die capacitance and packaging parameters.

Extracting the Data

Once the signals have been grouped appropriately, obtain the actual I-V curves and rise/fall times for output and I/O buffers. There are two ways to get this information:

- For pre-silicon models use circuit simulation tools to obtain the information over the worst cases of process and temperature variations, then to correlate the model against the actual silicon.
- When the actual silicon is available, use the data from physical measurements to build the model. However, it is difficult to get worst case min and max data over process and temperature this way.

OBTAINING CURVES BY SIMULATION

Use a simulator to obtain:

- The V-I data
- The rise/fall times

The general steps for aquiring this information follow.

Simulation Specifics

Analyze the I/O buffer cell and determine the input configuration for proper buffer operation. Specifically, configure the control inputs (pulled to a logic high or low) to enable the output transistors and to turn on each pull-up or pull-down device as required. For both the rise/fall time and I-V curve measurements, use "typical" process parameters.

For each rise time, fall time, pullup I-V curve and pull-down I-V curve measurement, use three sets of values: minimum (min), typical (typ), and maximum (max). Only typ is required, but it is highly recommended to supply the process corner information (min and max). The conditions required to obtain the min (slowest, weakest) and max (fastest, strongest) values are (from the IBIS specification):

- For CMOS:

  min = min V_{CC}, max temperature, typ process parameters
  max = max V_{CC}, min temperature, typ process parameters

- For bipolar:

  min = min V_{CC}, min temperature, typ process parameters
  max = max V_{CC}, max temperature, typ process parameters

To account for process variation, decrease the curent values taken at min conditions, increase the current values taken at max, and derate the rise and fall time values by the appropriate percentages. These percentages are determined either empirically or through simulation using fast and slow process files.

Rise and Fall Measurements

Obtain rise and fall time measurements by setting up the simulator for a transient analysis simulation. The control inputs of the buffer are set to enable the buffer outputs and a driving waveform is applied to

the buffer input. The output load circuit is defined in the IBIS specification section titled *Notes on Data Derivation*. During simulation:

- The slew rate of the driving waveform used to stimulate the buffer should be the internal slew rate of the technology.
- To avoid errors when trying to correlate later simulations with those used to extract rise/fall time information, use the same "time step" throughout the simulation and correlation procedure.
- The rise and fall time measurement are "no load" measurements; i.e., remove the package parameters (L/R/C) before doing the simulation.
- For rise time measurements, a non-reactive load resistance (usually 50 Ohms) is tied to 0 V; for fall time measurements, the load resistance is tied to V_{CC}. The intent is to measure the sourcing (or sinking) current and the turn-on time of the device (pullup or pulldown) actually enabled. For open drain or ECL type devices, measure the rise and fall times into the load resistor and voltage used by the manufacture when specifing propogation delays. The rise and fall time is defined as the time it takes the output to go from 20% to 80% of its final value.

  The "ramp rate" posted in an IBIS file is defined as:

$$\frac{dv}{dt} = \frac{20\% \text{ to } 80\% \text{ voltage swing}}{\text{Time it takes to swing the above voltage}}$$

I-V Characteristics

Obtain I-V characteristics for a buffer by setting the simulator for a DC sweep analysis (sometimes called a transfer function analysis). Set the control signals to enable the buffer and turn on either the pullup or pull-down transistor(s). Tie a voltage source to the output node and sweep it over the proper voltage range as defined in the IBIS specification (for standard output and I/O devices the range is from $-V_{CC}$ to $V_{CC} * 2$). To simplify the creation of the I-V tables it is permissable to use the same sweep range for all three (typ, min and max) conditions even though VCC itself had been adjusted.

If the ESD protection (power clamp or ground clamp) diodes are included as part of the circuit, disconnect them before performing the simulation so that the I-V curves are for the pullup and pull-down transistors only. Then reconnect the diodes, configure the buffer to disable the output, and perform the simulation again to obtain the diode I-V data.

Note:

The IBIS specification calls for the pullup and power clamp diode I-V data to be referenced to V_{CC}. To put the data into a table format properly, adjust the sweep voltage along with V_{CC}. For example, the sweep voltage for a 5 V part under typical conditions would range from -5 V to +10 V. For minimum conditions, where the V_{CC} was adjusted to 4.75 V, the sweep voltage would also have to be adjusted -0.25 V, to sweep from -5.25 V to +9.75 V. Likewise, for maximum conditions, adjust the sweep voltage positive along with the V_{CC}. As mentioned above, the 15V sweep RANGE can remain the same for all three simulations.

OBTAINING CURVES BY LAB MEASUREMENTS OF SILICON

You can obtain I-V curves and rise/fall time information from the actual IC, using the following lab setup:

- A programmable power supply with an output capable of sinking and sourcing current while maintaining the required output voltage. The output must be floating.
- A curve tracer
- A digital sampling oscilloscope with at least a 4 GHz bandwidth
- A low capacitance probe, e.g. FET
- A test fixture used for DC measurements
- A motherboard or specific test fixture used for AC measurements
- If available, a thermoelectronic hot/cold plate (a peltier device), to control die temperature

To obtain I-V curve measurements, mount the device under test (DUT) in the DC test fixture and connect the power and ground pins of the DUT to the programmable power supply. Attach the hot/cold plate to the device with a very thin layer of thermal grease and adjust the temperature as desired. Wait for the die to stabilize at the desired temperature. Select an output on the DUT in the desired state (high or low) and use the curve tracer to obtain the I-V characteristics of the output.

Notes

During curve tracing of a tri-statable output, the curve contains both the transistor and the diode output characteristics. To obtain curves for the diodes alone, select and curve trace the output in its high impedance state.

Devices containing time-delayed feedback can produce bad results.

Reference the pullup and power clamp data to V_{CC}, as described in the IBIS specification. You can obtain this data directly by connecting the curve tracer's negative (reference) lead to the V_{CC} supply of the DUT, then setting the curve tracer for a negative sweep. Make sure no ground path connects back through the AC line between the device ground and power supply ground. For standard pulldown and clamp diode curves, attach the negative lead to the DUT's GND supply and use a positive sweep direction. Ensure the supply is floating.

Note that the curve tracer may not be able to sweep the entire range required by the IBIS specifcation. In this case the modeler must extrapolate the curves to the required range.

Capturing rise/fall time data requires either a specific test fixture or a motherboard to which the DUT can be attached. Rise/fall time measurements require an oscilloscope with at least a 4 GHz bandwidth. Take into account the effect on the rise/fall times of the device packaging and capacitive load. Use a probe with extremely low loading, i.e. 1 pf or less, such as a FET probe. The probe grounding should be less than 0.5 inches; i.e., don't use the standard 6 inch probe grounds.

Take an oscilloscope picture of a buffer driving a known load. Then, using the known packaging parameters and measured I-V curves, construct a simulation model of the device using a best guess of the rise/fall time. With an IBIS simulator, adjust the rise/fall times in the model until the simulation results match the oscilloscope waveforms. For greater control, lift the pin under test from any load other than the scope probe and simulate with a package and probe model.

Putting the Data Into an IBIS File

Enter the I-V data into four tables: one each for pullup, pulldown, ground clamp, and power clamp. Specific information on creating the IBIS file is given later in this document. To construct the I-V tables:

1. The pullup and power clamp voltage points are referenced to V_{CC}. Enter these points into the tables using the formula:

   Vtable = V_{CC} - Voutput

   For example, enter the data point of a standard 5V device with a pullup sourcing 10 mA at 4 V into the pullup table as (5 V - 4 V), i.e.:

   Vtable = 5 V - 4 V
   = 1 V

2. Most simulators extrapolate the last two data points in a table to calculate values beyond the table's range. Therefore, be sure that all curves going to zero have the last two data points as zero. As an example, the **incorrect** way to enter a diode curve is:

Voltage	**Current**
0.0 V	0 mA
0.6 V	2 mA

   With the above, a simulator assumes a -2 mA current through the diode at -.6 V bias. The **correct** way to enter the curve is:

Voltage	**Current**
0.0 V	0 mA
0.4 V	0 mA
0.6 V	2 mA

   With this table, the simulator extrapolates the diode curve correctly.

3. When the pullup/pullown I-V data contains clamp diode current data, the diode data must be separated from the pullup/pulldown data. Generally, this involves subracting the clamp diode data (obtained while the device is in tri-state) from the “on” state pullup/pulldown curves. For an output-only device where separate diode clamp curves are not available, you need supply only the pullup/pulldown curves.

CREATING AN IBIS FILE

The formal IBIS standard is included as the last section of this document. The specification goes into great detail on how to construct the file.

After creating an IBIS file, check it for correct construction and syntax. A program called "ibis_chk" is used to verify the IBIS file. This program (the golden parser) is also available from the IBIS Open Forum (see the section titled *Resources*). The golden parser is available for a variety of hardware platforms and operating systems.

To run the golden parser at the prompt, type:

ibis_chk <filename>

Note

There are two versions of this program: one for DOS based systems and one for UNIX based systems. Because of the differences in line feed/carriage return characters in DOS and UNIX, an IBIS file created with a DOS text editor can fail when checked with the UNIX version of the program. Utilities such as "dos2unix" and "unix2dos" are available to convert between the DOS and UNIX texts.

Validating the Model

Once an IBIS model has been created, it must be validated. Validation involves

1. From the IBIS data, creating a behavioral simulation model in a target simulator that supports IBIS.

2. Running the model with standard loads.

3. Comparing the results against a transistor-level reference simulation using the same loads.

You can use any simulator that supports IBIS. Contact the simulator vendor and request their parser, converter, or application note on using IBIS models on their tools. To find simulator vendors that support IBIS, see the IBIS member list maintained in the "vhdl.org" archives.

Correlating the Data

The last step in the modeling process is to correlate the simulation results with actual silicon measurements. To obtain I-V curves and rise/fall time measurements, see the section titled *Obtaining Curves by Lab Measurement of Silicon*.

Correlation involves measuring the I-V curves and rise/fall times of an actual IC and verifying that they fall within the maximum and minimum values used in the IBIS model. In addition, for ICs in a motherboard or other test setup driving a known load, compare the oscilloscope waveforms with simulation waveforms using the same load.

Note

The oscilloscope adds a load to the circuit and the response of the oscilloscope affects the response measured.

EXAMPLE 1: IBIS DATA FILE

```
[IBIS Ver]      1.0                     | Used for template variations
[Comment char]  |_char
[File name]     ver1_1.ibs
[File Rev]      1.0                             | Used for .ibs file variations
[Date]          04/19/93                        | Latest file revision date
[Source]        Put originator and source of information here.  For example:
                From silicon level SPICE model at Intel,
                From lab measurement at IEI,
                Compiled from manufacturer's data book at Quad Design, etc.
[Notes]         This section can be used for any special notes related
                to the file.
[Disclaimer]    This information is for modeling purposes only, and
                is not guaranteed.              | May vary by component
[Component]     Component Name
[Manufacturer]  Manufacturer's Name             | e.g., Intel
[Package]
| variable      typ             min             max
R_pkg           250.0m          225.0m          275.0m
L_pkg           15.0nH          12.0nH          18.0nH
C_pkg           18.0pF          15.0pF          20.0pF
[Pin]   signal_name     model_name      R_pin   L_pin   C_pin
|
  1     RAS0#           Buffer1         200.0m  5.0nH   2.0pF
  2     RAS1#           Buffer2         209.0m  NA      2.5pF
  3     EN1#            Input1          NA      6.3nH   NA
  4     A0              3-state
  5     D0              I/O1
  6     RD#             Input2          310.0m  3.0nH   2.0pF
  7     WR#             Input2
  8     A1              I/O2
  9     D1              I/O2
 10     GND             GND             297.0m  6.7nH   3.4pF
 11     RDY#            Input2
 12     GND             GND             270.0m  5.3nH   4.0pF
|  .
|  .
|  .
 18     VCC3            POWER
 19     NC              NC
 20     Vcc5            POWER           226.0m  NA      1.0pF
[Model]         model_name
Model_type      Input, Output, I/O, 3-state, Open_drain | List one only
Polarity        Non-Inverting, Inverting                | List one only, if any
Enable          Active-High, Active-Low                 | List one only, if any
| Signals       RAS, CAS, A(0-64), D(0-128),...         | Local list, if desired
Vinl = 0.8V                             | input logic "low" DC voltage, if any
Vinh = 2.0V                             | input logic "high" DC voltage, if any
| variable      typ             min             max
C_comp          12.0pF          10.0pF          15.0pF
[Voltage range]         5.0V            4.5V            5.5V
[Pulldown]
|  Voltage   I(typ)    I(min)    I(max)
|
   -5.0V    -40.0m    -34.0m    -45.0m
   -4.0V    -39.0m    -33.0m    -43.0m
|    .
|    .
    0.0V      0.0m      0.0m      0.0m
|    .
|    .
    5.0V     40.0m     34.0m     45.0m
   10.0V     45.0m     40.0m     49.0m
|
[Pullup]
|
|  Voltage   I(typ)    I(min)    I(max)
|
   -5.0V     32.0m     30.0m     35.0m
   -4.0V     31.0m     29.0m     33.0m
```

```
|     .
|     .
|    0.0V      0.0m      0.0m      0.0m
|     .
|     .
|    5.0V    -32.0m    -30.0m    -35.0m
|   10.0V    -38.0m    -35.0m    -40.0m
|
[GND_clamp]
|
|  Voltage   I(typ)    I(min)    I(max)
|
   -5.0V  -3900.0m  -3800.0m  -4000.0m
   -0.7V    -80.0m    -75.0m    -85.0m
   -0.6V    -22.0m    -20.0m    -25.0m
   -0.5V     -2.4m     -2.0m     -2.9m
   -0.4V      0.0m      0.0m      0.0m
    5.0V      0.0m      0.0m      0.0m
|
[POWER_clamp]
|
|  Voltage   I(typ)    I(min)    I(max)
|
   -5.0V   4450.0m        NA        NA
   -0.7V     95.0m        NA        NA
   -0.6V     23.0m        NA        NA
   -0.5V      2.4m        NA        NA
   -0.4V      0.0m        NA        NA
    0.0V      0.0m        NA        NA
[End]
```

Resources

The IBIS Open Forum is an industry-wide forum that controls the official IBIS specification. Minutes of IBIS meetings, email correspondence, proposals for specification changes, etc. are on-line at "vhdl.org". To join in the email discussions, send a message to "ibis-request@vhdl.org" and request that your name be added to the IBIS mail reflector. Be sure to include your email address.

To download a copy of the specification, the golden parser, various public-domain models, the *IBIS Overview* in PostScript, and other information, either phone in by modem or use FTP.

FTP: (IP address 198.31.14.3)
login as "anonymous"
password is your email address

Modem: (408)945-4170
login as "guest"
password is your email address

IBIS-related files are in the directory "/pub/ibis" and its subdirectories.

To get documents by email, send an email message to "archive@vhdl.org" with the following commands in the message body:

path <your_email_address>
send docs <name_of_document>

For direct modem access, dial-up to the vhdl.org system at (408) 945-4170. You can use any baud rate up to 14,400, any parity, start and stop bits, and any v.* settings. Log in using the "guest" account. Simple UNIX commands such as "cd", "ls", and "cat" are available and you can download files using "kermit", "zmodem", or "sz" (another zmodem application).

For Internet access, use "ftp vhdl.org" (or "ftp 198.31.14.3") and log in as user "anonymous". The gopher utility is available and highly recommended. Gopher to "vhdl.org". Set "binary" mode for transferring binary files (*.doc, *.fm, *.xls).

The IBIS specification and overview are also available from Intel's AMO APPS BBS, via modem dial-up to (916) 356-3600.

IBIS V1.1

```
|================================================================================
| Statement of Intent:
|
| In order to enable an industry standard method to electronically transport
| IBIS Modeling Data between silicon vendors, simulation software vendors, and
| end customers, this template is proposed.  The intention of this template is
| to specify a consistent format that can be parsed by software, allowing each
| simulation vendor to derive models compatible with their own product.
|
| One goal of this template is to represent the current state of IBIS data,
| while allowing a growth path to more complex models / methods (when deemed
| appropriate).  This would be accomplished by a revision of the base
| template, and possibly the addition of new keywords or categories.
|
| Another goal of this template is to ensure that it is simple enough for
| silicon vendors and customers to use and modify, while ensuring that it is
| rigid enough for software simulation vendors to write reliable parsers.
|
| Finally, this template is meant to contain a complete description of the I/O
| elements on an entire component.  Consequently, several models will need to
| be defined in each file, as well as a table that equates the appropriate
| buffer to the correct pin and signal name.
|
| Version 1.1 of this electronic template was finalized by an industry-wide
| group of simulation experts representing various companies and interests.
| "IBIS Open Forum" meetings were held biweekly to accomplish this task.
|
| Commitment to Backward Compatibility.  Version 1.0 is the first valid IBIS
| ASCII file format.  It represents the minimum amount of I/O buffer
| information required to create an accurate IBIS model of common CMOS and
| bipolar I/O structures.  Future revisions of the ASCII file will add items
| considered to be "enhancements" to Version 1.0 to allow accurate modeling
| of new, or other, I/O buffer structures.  Consequently, all future
| revisions will be considered super sets of Version 1.0, allowing backward
| compatibility.  In addition, as modeling platforms develop support for
| revisions of the IBIS ASCII template, all previous revisions of the
| template must also be supported.
|
| Version 1.1 update.  The file "ver1_1.ibs" is conceptually the same as
| the 1.0 version of the IBIS ASCII format (ver1_0.ibs).  However, various
| comments have been added for further clarification.
|
|================================================================================
|
| General syntax rules and guidelines:
|
| 1)  The content of the IBIS_ASCII file is case sensitive, except for file
| names, reserved words and keywords.  Reserved words and keywords are not
| case sensitive, and file names must be all lower case.
|
| 2)  The following words are reserved words and must not be used for
|     any other purposes in the document:
|        POWER - reserved model name, used with power supply pins,
|        GND   - reserved model name, used with ground pins,
|        NC    - reserved model name, used with no connect pins,
|        NA    - used where data not available.
|
| 3)  File names used in the IBIS_ASCII file must only have lower case
| characters to enhance UNIX compatibility and must conform to DOS rules.
| (The length of a file name should not exceed eight plus three characters
| and it must not contain special characters which are illegal in DOS).
|
| 4)  The IBIS_ASCII file must have no more than 80 characters per line.
|
| 5)  Anything following the comment character is ignored and considered a
| comment on that line.  The default "|" (pipe) character can be changed by
| the keyword [Comment char] to any other character.  The [Comment char]
| keyword can be used throughout the file as desired.
|
| 6)  Keywords must be enclosed in square brackets, [], and must start in
| column 1 of the line.
|
| 7)  Valid scaling factors are:
|       M = mega, k = kilo, m = milli, u = micro, n = nano, p = pico.
| When no scaling factors are specified, the appropriate base units are
| assumed.  (These are Volts, Amperes, Ohms, Farads and Henries).  The parser
| will look at only one alphabetic character after a numerical entry,
| therefore it is enough to use only the prefixes to scale the parameters.
```

```
| However, for clarity, it is allowed to use full abbreviations for the          |
| units.  (e.g., pF, nH, mA, mOhm).  In addition, scientific notation IS         |
| allowed (e.g., 1.2345e-12).                                                    |
|                                                                                |
| 8)  The V/I data tables should use enough data points around sharply curved    |
| areas of the V/I curves to describe the curvature accurately.  In linear       |
| regions there is no need to define unnecessary data points.                    |
|                                                                                |
| 9)  Currents are considered positive when their direction is into the          |
| component.                                                                     |
|                                                                                |
|================================================================================|
|     Keyword:  [IBIS Ver]                                                       |
|    Required:  Yes                                                              |
| Description:  Used to specify the IBIS ASCII template version.  This will be   |
|               used to inform an electronic parser of the kinds of data types   |
|               that will be present in the file.                                |
| Usage Rules:  [IBIS Ver] must be the first keyword in any IBIS file.  It is     |
|               normally on the first line of the file, but can be preceded      |
|               by comment lines (that must begin with a "|").                   |
|--------------------------------------------------------------------------------|
|[IBIS Ver]     1.1                     | Used for template variations           |
|================================================================================|
|     Keyword:  [Comment char]                                                   |
|    Required:  Optional                                                         |
| Description:  Used to define a new comment character to replace the default    |
|               "|" (pipe), if desired.                                          |
| Usage Rules:  The new comment character which is to be defined must be         |
|               followed by the underscore character and the letters "char".     |
|               For example: "|_char" redundantly redefines the comment         |
|               character to be the pipe character.  The new comment character  |
|               will be in effect only following the [Comment char] keyword.    |
|               The following characters can NOT be used:  A B C D E F G H I J   |
|               K L M N O P Q R S T U V W X Y Z a b c d e f g h i j k l m n o     |
|               p q r s t u v w x y z 0 1 2 3 4 5 6 7 8 9 [ ] . _ / =           |
| Other Notes:  The [Comment char] keyword can be used throughout the file, as   |
|               desired.                                                         |
|--------------------------------------------------------------------------------|
|[Comment char]  |_char                                                          |
|================================================================================|
|     Keyword:  [File name]                                                      |
|    Required:  Yes                                                              |
| Description:  Used to specify the name of the IBIS file, "filename.ibs".       |
| Usage Rules:  The file name must comply with normal DOS rules (8 char. max.    |
|               and no characters that are illegal in DOS).  In addition, it     |
|               must be all lower case, and use the extension ".ibs".            |
|--------------------------------------------------------------------------------|
|[File name]    ver1_1.ibs                                                       |
|================================================================================|
|     Keyword:  [File Rev]                                                       |
|    Required:  Yes                                                              |
| Description:  Used to track the revision level of a particular .ibs file.      |
| Usage Rules:  Revision level can be set at the discretion of the engineer      |
|               defining the file.  The following guidelines are recommended:    |
|                       0.x     silicon and file in development                  |
|                       1.x     pre-silicon file data from silicon model only    |
|                       2.x     file correlated to actual silicon measurements   |
|                       3.x     mature product, no more changes likely           |
|--------------------------------------------------------------------------------|
|[File Rev]     1.0                          | Used for .ibs file variations   |
|================================================================================|
|    Keywords:  [Date] [Source] [Notes] [Disclaimer]                             |
|    Required:  Optional                                                         |
| Description:  Optionally used for further file clarifications.                 |
| Usage Rules:  The [Date] information is allowed to contain blanks, and be of   |
|               any format up to 40 characters.                                  |
|--------------------------------------------------------------------------------|
|[Date]         04/19/93                     | Latest file revision date       |
|[Source]       Put originator and source of information here.  For example:     |
|               From silicon level SPICE model at Intel,                         |
|               From lab measurement at IEI,                                     |
|               Compiled from manufacturer's data book at Quad Design, etc...    |
|[Notes]        This section can be used for any special notes related           |
|               to the file.                                                     |
|[Disclaimer]   This information is for modeling purposes only, and              |
|               is not guaranteed.           | May vary by component             |
|================================================================================|
|     Keyword:  [Component]                                                      |
|    Required:  Yes                                                              |
| Description:  Used to mark the beginning of the IBIS description of the        |
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|                integrated circuit named after the keyword.                  |
|  Usage Rules:  If the .ibs file contains data for more than one component,  |
|                each section must begin with a new [Component] keyword.  The |
|                length of the Component Name must not exceed 40 characters,  |
|                and blank characters are allowed.                            |
|-----------------------------------------------------------------------------|
[Component]     Component Name
|=============================================================================|
|      Keyword:  [Manufacturer]                                               |
|     Required:  Yes                                                          |
|  Description:  Used to clarify the component's manufacturer.                |
|  Usage Rules:  The length of the Manufacturer's Name must not exceed 40     |
|                characters (blank characters are allowed, e.g., Texas        |
|                Instruments).  In addition, each manufacturer must use a     |
|                consistent name in all .ibs files.                           |
|-----------------------------------------------------------------------------|
[Manufacturer]  Manufacturer's Name             | e.g., Intel
|=============================================================================|
|      Keyword:  [Package]                                                    |
|     Required:  Yes                                                          |
|  Description:  Used to define a range of values for the default packaging   |
|                resistance, inductance, and capacitance of the component pins.|
|  Sub-Params:   R_pkg, L_pkg, C_pkg                                          |
|  Usage Rules:  Typical column must be specified.  If data for the other     |
|                columns are not available, they must be noted with "NA".     |
|  Other Notes:  If RLC parameters are available for individual pins, they can|
|                be listed in columns 4-6 under keyword [Pin].  The values    |
|                listed in the [Pin] description section override the default |
|                values defined here.                                         |
|-----------------------------------------------------------------------------|
[Package]
| variable      typ             min             max
R_pkg           250.0m          225.0m          275.0m
L_pkg           15.0nH          12.0nH          18.0nH
C_pkg           18.0pF          15.0pF          20.0pF
|=============================================================================|
|      Keyword:  [Pin]                                                        |
|     Required:  Yes                                                          |
|  Description:  Used to associate the component's I/O models to its various  |
|                external pins and signal names.                              |
|   Sub-Params:  signal_name, model_name, R_pin, L_pin, C_pin                 |
|  Usage Rules:  All pins on a component must be specified.  The first column |
|                must contain the pin name.  The second column, signal_name,  |
|                gives the data book name for the signal on that pin.  The    |
|                third column, model_name, associates the I/O model for that |
|                pin.  Each model_name must have a [Model] keyword below,     |
|                unless it is a reserved model name (POWER, GND, or NC).      |
|                                                                             |
|                Each line must contain either three or six columns.  A pin   |
|                line with three columns only associates the pin's signal and |
|                model.  Six columns can be used to override the default      |
|                package values (specified under [Package]) FOR THAT PIN ONLY.|
|                When using six columns, the headers R_pin, L_pin, and C_pin  |
|                must be listed.  If "NA" is in columns 4 through 6, the      |
|                default packaging values must be used.                       |
|                                                                             |
|                Column length limits are:                                    |
|                        [Pin]            5 characters max                    |
|                        model_name      20 characters max                    |
|                        signal_name     20 characters max                    |
|                        R_pin            9 characters max                    |
|                        L_pin            9 characters max                    |
|                        C_pin            9 characters max                    |
|-----------------------------------------------------------------------------|
[Pin]   signal_name     model_name      R_pin   L_pin   C_pin
|
  1     RAS0#           Buffer1         200.0m  5.0nH   2.0pF
  2     RAS1#           Buffer2         209.0m  NA      2.5pF
  3     EN1#            Input1          NA      6.3nH   NA
  4     A0              3-state
  5     D0              I/O1
  6     RD#             Input2          310.0m  3.0nH   2.0pF
  7     WR#             Input2
  8     A1              I/O2
  9     D1              I/O2
 10     GND             GND             297.0m  6.7nH   3.4pF
 11     RDY#            Input2
 12     GND             GND             270.0m  5.3nH   4.0pF
|  .
|  .
```

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|  .
 18     VCC3            POWER
 19     NC              NC
 20     Vcc5            POWER           226.0m  NA      1.0pF
|================================================================================|
|     Keyword:  [Model]                                                          |
|    Required:  Yes                                                              |
| Description:  Used to define a model, and its attributes.                      |
|  Sub-Params:  Model_type, Polarity, Enable, Vinl, Vinh, C_comp                 |
| Usage Rules:  Each Input, Output, I/O, 3-state, or Open-drain model must       |
|               begin with the keyword [Model].  The model_name must match       |
|               the one that is listed under the [Pin] keyword and must not     |
|               contain more than 20 characters.  An .ibs file must contain     |
|               enough [Model] keywords to cover all of the model_names         |
|               specified under the [Pin] keyword, except for those             |
|               model_names which use reserved words (POWER, GND and NC).       |
|               Model_names with reserved words are an exception and            |
|               they do not have to have a corresponding [Model] keyword.       |
|               C_comp is allowed to use "NA" for the min and max values only.   |
| Other Notes:  A complete [Model] description normally contains the following  |
|               keywords:  [Voltage range], [Pullup], [Pulldown], [GND_clamp],  |
|               [POWER_clamp], and [Ramp].  However, some models may have only   |
|               a subset these keywords.  For example, an input structure       |
|               normally only needs the [Voltage range], [GND_clamp], and       |
|               possibly the [POWER_clamp] keywords.                            |
|               Note that C_comp defines the silicon die capacitance.  This      |
|               value should not include the capacitance of the package.        |
|                                                                                |
|--------------------------------------------------------------------------------|
[Model]         model_name
Model_type      Input, Output, I/O, 3-state, Open_drain | List one only
Polarity        Non-Inverting, Inverting                | List one only, if any
Enable          Active-High, Active-Low                 | List one only, if any
| Signals       RAS, CAS, A(0-64), D(0-128),...         | Local list, if desired
Vinl = 0.8V                             | input logic "low" DC voltage, if any
Vinh = 2.0V                             | input logic "high" DC voltage, if any
| variable      typ             min             max
C_comp          12.0pF          10.0pF          15.0pF
|================================================================================|
|     Keyword:  [Voltage range]                                                  |
|    Required:  Yes                                                              |
| Description:  Used to define the power supply voltage tolerance over which    |
|               the model is intended to operate.                                |
| Usage Rules:  Actual voltages (not percentages) are to be presented in the     |
|               usual typ, min, max format.  "NA" is allowed for the min and     |
|               values only.                                                     |
| Other Notes:  [Voltage range] also describes the voltage range over which      |
|               the various V/I curves and ramp rates were derived.              |
|--------------------------------------------------------------------------------|
| variable              typ             min             max
[Voltage range]         5.0V            4.5V            5.5V
|================================================================================|
|    Keywords:  [Pulldown], [Pullup], [GND_clamp], [POWER_clamp]                 |
|    Required:  Yes, if they exist in the device                                 |
| Description:  The data points under these keywords define the V/I curves of   |
|               the pulldown and pullup structures of an output buffer and the  |
|               V/I curves of the clamping diodes connected to the GND and the  |
|               POWER pins, respectively.                                        |
| Usage Rules:  In each of these sections the first column contains the          |
|               voltage value, and the three remaining columns hold the         |
|               typical, minimum, and maximum current values.   The four        |
|               entries, Voltage, I(typ), I(min), and I(max) must be placed on  |
|               a single line and must be separated by at least one white       |
|               space or tab character.                                         |
|               All four columns are required under these keywords, however     |
|               data is only required in the typical column.  If minimum        |
|               and/or maximum current values are not available, the reserved    |
|               word "NA" must be used.  "NA" can be used for currents in the    |
|               typical column, but numeric values MUST be specified for the    |
|               first and last voltage points on any V/I curve.  Each V/I        |
|               curve must have at least 2, but not more than 100, voltage       |
|               points.                                                         |
| Other Notes:  It should be noted that the V/I curve of the [Pullup] and the    |
|               [POWER_clamp] structures are 'Vcc relative', meaning that the   |
|               voltage values are referenced to the Vcc pin.  The voltages in  |
|               the data tables are derived from the equation:                   |
|                       Vtable = Vcc - Voutput                                   |
|               Therefore, for a 5V component, -5 V in the table actually       |
|               means 5 V above Vcc, which is +10 V with respect to ground;     |
|               and 10 V means 10 V below Vcc, which is -5 V with respect to    |
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|               ground.  Vcc-relative data is necessary to model a pullup      |
|               structure properly, since the output current of a pullup       |
|               structure depends on the voltage between the output and Vcc    |
|               pins and not the voltage between the output and ground pins.   |
|               Note that the [GND_clamp] V/I curve can include quiescent      |
|               input currents, or the currents of a 3-stated output if so     |
|               desired.                                                       |
|------------------------------------------------------------------------------|
[Pulldown]
|  Voltage   I(typ)    I(min)    I(max)
|
   -5.0V    -40.0m    -34.0m    -45.0m
   -4.0V    -39.0m    -33.0m    -43.0m
|    .
|    .
    0.0V      0.0m      0.0m      0.0m
|    .
|    .
    5.0V     40.0m     34.0m     45.0m
   10.0V     45.0m     40.0m     49.0m
|
[Pullup]
|
|  Voltage   I(typ)    I(min)    I(max)
|
   -5.0V     32.0m     30.0m     35.0m
   -4.0V     31.0m     29.0m     33.0m
|    .
|    .
    0.0V      0.0m      0.0m      0.0m
|    .
|    .
    5.0V    -32.0m    -30.0m    -35.0m
   10.0V    -38.0m    -35.0m    -40.0m
|
[GND_clamp]
|
|  Voltage   I(typ)    I(min)    I(max)
|
   -5.0V  -3900.0m  -3800.0m  -4000.0m
   -0.7V    -80.0m    -75.0m    -85.0m
   -0.6V    -22.0m    -20.0m    -25.0m
   -0.5V     -2.4m     -2.0m     -2.9m
   -0.4V      0.0m      0.0m      0.0m
    5.0V      0.0m      0.0m      0.0m
|
[POWER_clamp]
|
|  Voltage   I(typ)    I(min)    I(max)
|
   -5.0V   4450.0m       NA        NA
   -0.7V     95.0m       NA        NA
   -0.6V     23.0m       NA        NA
   -0.5V      2.4m       NA        NA
   -0.4V      0.0m       NA        NA
    0.0V      0.0m       NA        NA
|==============================================================================|
|     Keyword:  [Ramp]                                                         |
|    Required:  Yes, except for inputs                                         |
| Description:  Used to define the rise and fall times of a buffer.            |
|  Sub-Params:  dV/dt_r, dV/dt_f                                               |
| Usage Rules:  These parameters describe an ideal slope and can be expressed  |
|               as a ratio of any reasonable voltage and time values as shown  |
|               in the examples.  The [Ramp] values are allowed to use "NA"    |
|               for the min and max values only.                               |
|------------------------------------------------------------------------------|
[Ramp]
| variable      typ             min             max
dV/dt_r         4.2/1.8n        3.5/2.5n        5.0/1.1n
dV/dt_f         2.5/1.5n        2.0/2.3n        3.0/0.8n
|==============================================================================|
|     Keyword:  [End]                                                          |
|    Required:  Yes                                                            |
| Description:  Used to define the end of the .ibs file.                       |
|------------------------------------------------------------------------------|
[End]
|==============================================================================|
|                        NOTES ON DATA DERIVATION METHOD                       |
|                                                                              |
| This section explains how data values are derived.  The intention here is to |
```

avoid over-guardbanding, enabling simulation results that are meaningful and useful. This is accomplished by having each silicon vendor base their data on typical process data, and then derate by voltage and temperature, and a proprietary "X%" factor. This methodology also has the nice feature that the data can be derived either from vendor-proprietary silicon models, or typical device measurement over temperature/voltage.

1) V/I curves for CMOS devices:
   typ = nominal voltage, 50 degrees C, typical process
   min = low voltage tol, 100 degrees C, typical process, minus "X%"
   max = hi voltage tol, 0 degrees C, typical process, plus "X%"

   V/I curves for bipolar devices:
   typ = nominal voltage, 50 degrees C, typical process
   min = low voltage tol, 0 degrees C, typical process, minus "X%"
   max = hi voltage tol, 100 degrees C, typical process, plus "X%"

   where X% should be statistically determined by the silicon vendor based on numerous fab lots, test chips, process controls, ... The value of X need not be published in the IBIS file, and may decrease over time as data on the I/O buffers and silicon process increases. Temperatures are junction temperatures.

2) Voltage Ranges:
   Points for each curve must span the voltages listed below:

Curve	Low Voltage	High Voltage
[Pulldown]	GND - POWER	POWER + POWER
[Pullup]	GND - POWER	POWER + POWER
[GND_clamp]	GND - POWER	GND + POWER
[POWER_clamp]	POWER	POWER + POWER

   For example, a device with a 5 V power supply voltage should be characterized between (0 - 5) = -5 V and (5 + 5) = 10 V; and a device with a 3.3 V power supply should be characterized between (0 - 3.3) = -3.3 V and (3.3 + 3.3) = 6.6 V for the pulldown curve.

3) Ramp Rates:
   The ramp rates (listed in AC characteristics below) should be derived by:
   1. Start with silicon model, remove all packaging.
   2. Attach 50 Ohm resistor to GND to derive rising edge ramp.
   3. Attach 50 Ohm resistor to POWER to derive falling edge ramp.
   4. Due to the resistor, output swings will not make a full transition as expected. However the pertinent data can still be collected as follows:
      a) determine the 20% to 80% voltages of the 50 Ohm swing
      b) measure this voltage change as "dv"
      c) measure the amount of time required to make this swing "dt"
   5. Post the value as a ratio "dv/dt", the simulation tool vendor will extrapolate this value to span the required voltage swing range in the final model.
   6. Typ, Min, and Max must all be posted, and are derived at the same extremes as the V/I curves, which are:

   Ramp times for CMOS devices:
   typ = nominal voltage, 50 degrees C, typical process
   min = low voltage tol, 100 degrees C, typical process, minus "Y%"
   max = hi voltage tol, 0 degrees C, typical process, plus "Y%"

   Ramp times for bipolar devices:
   To be determined by manufacturer.

   Note that the derate factor, "Y%", may be different than that used for the V/I curve data. This factor is similar to the X% factor described above. As in the case of V/I curves, temperatures are junction temperatures here also.

   7. The rise time of an open-drain device must be measured into a 50 Ohm pullup resistor tied to the power pin.

It is expected that this data will be created from silicon vendor proprietary silicon-level models, and later correlated with actual device measurement.