IBIS: I/O Buffer Information Specification Overview

Version 1.0
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Intel Corporation

IBIS (Input/Output Buffer Information Specification) is an emerging standard for electronic behavioral specification of integrated circuit (IC) input/output (I/O) analog characteristics. IBIS specifies a consistent software-parsable format for essential behavioral information. With IBIS, simulation tool vendors can accurately model compatible buffers. The goal of IBIS is to support all simulators of all degrees of sophisitication.

Advantages of IBIS

IBIS provides advantages over previous I/O buffer model development methodologies in information protection, performance, accuracy, time to market, and industry compatibility.

Protection

Previous methodologies used the actual circuit designs and revealed detailed, sensitive information about both the buffer design and the underlying fabrication processes. IBIS relies on tabulated voltage versus current (V/I) characteristics, timing characteristics, and package information, thus protecting vendor intellectual property. This approach is designed to provide models that reveal no proprietary information about the design or process technology.

Performance and Accuracy

The behavioral IBIS simulations run much faster than any corresponding structural (e.g., silicon) models. Speed-ups of 25X are common. No accuracy is sacrificed, since the V/I methodology takes into account many non-linear aspects of the I/O design, such as package parasitics and forward-biased ESD protection diode effects.

Time to Market and Industry Compatibility

As market pressures shorten the design cycle, the design engineers need earlier availability of the models. At the same time, faster system designs result in more complex and less forgiving design issues. The IBIS modeling data can be derived from circuit simulation or measured on a curve tracer or oscilloscope. By using such data sources, semiconductor vendors can provide accurate I/O buffer models with or before the first component availability. In addition, any model created using IBIS format is compatible with virtually all industry-wide simulation platforms.

History and Contact Information

IBIS was first developed at Intel Corporation and has been expanded to its current form through the cooperative efforts of twenty additional analog simulator vendors, computer manufacturers and IC vendors. The first revision of IBIS_ASCII Standard has been ratified by these companies:

Cadence Design Systems	Intel Corporation	Mentor Graphics Corporation
Quantic Laboratories	HyperLynx	Contec Microelectronics U.S.A. Inc.
MicroSim Corporation	Meta-Software	North Carolina State University
Integrity Engineering	IntuSoft	Quad Design Technology
Interconnectix, Inc.	Anacad	Logic Modeling Corporation
Zeelan Technology, Inc.	AnSoft Corporation	Performance Signal Integrity

IBIS information is available on-line via Internet email, anonymous ftp, and a number of BBS including CompuServe:

- Use either anonymous login or anonymous ftp (with no password) on the VHDL International BBS, (408)945-4170. Documentation resides in vhdl.org in the pub/ibis directory.
- To get on the IBIS Forum email list, send a request to ibis-request@vhdl.org.
- For copies of past mailings and other files, send a request to archive@vhdl.org. You can get a list of available documentation by sending such a request with a blank subject line and the following line in the message body:

  path <*your_email_address*>

For more information, contact Jon Powell at Quad Design at (805) 988-8250 or jonp@qdt.com.

Developing IBIS Capability

A variety of resources are available for developing IBIS compatible models and for verifying your model construction and syntax against IBIS.

Golden Parser for Developing and Checking Model Generators

Version 1.1 of the IBIS Golden Parser (ibis_chk) is available for checking model syntax against IBIS. This parser is also used by IBIS forum member companies to create simulator-specific IBIS data model generators. The behavior of model generators based on the Golden Parser varies insignificantly between simulators.

The Golden Parser is freely available in object code format for several platforms. Send email to ibis-request@vhdl.org.

You can also license the Golden Parser source code from the IBIS Forum. Contact Will Hobbs of Intel Corporation at (503) 696-4369, fax (503) 696-4210, e-mail hobbswil@ccm.hf.intel.com.

Technical Basis of IBIS

For simulating I/O interconnects, participating IC vendors offer detailed descriptions of their drivers and receivers, organized into machine-parsable ASCII files. Each such file provides the information needed to model all the buffers for a component.

At the end of this document are a portion of a sample IBIS file and a copy of the IBIS V1.1 Specification which contains explanations of all the formating, fields, and keywords.

A customer or IC vendor can put data into an IBIS file to be used as input for a broad range of simulation packages. Such simulation packages can interpret the IBIS data either directly or using a translator from an EDA vendor. In other formats, the same data can be used under SPICE packages for behavioral elements such as voltage-controlled current sources to model the pull-up, pull-down, and clamp characteristics of a given buffer.

Figure 1 shows the basic five elements that must be included for IBIS modeling of an I/O structure. Figure 2 shows an example block diagram for an IBIS behavioral model.

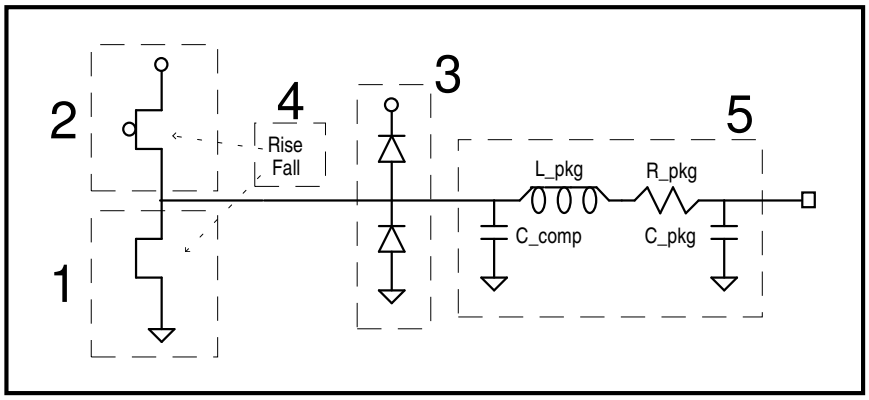


Figure 1: Elements of an IBIS Model

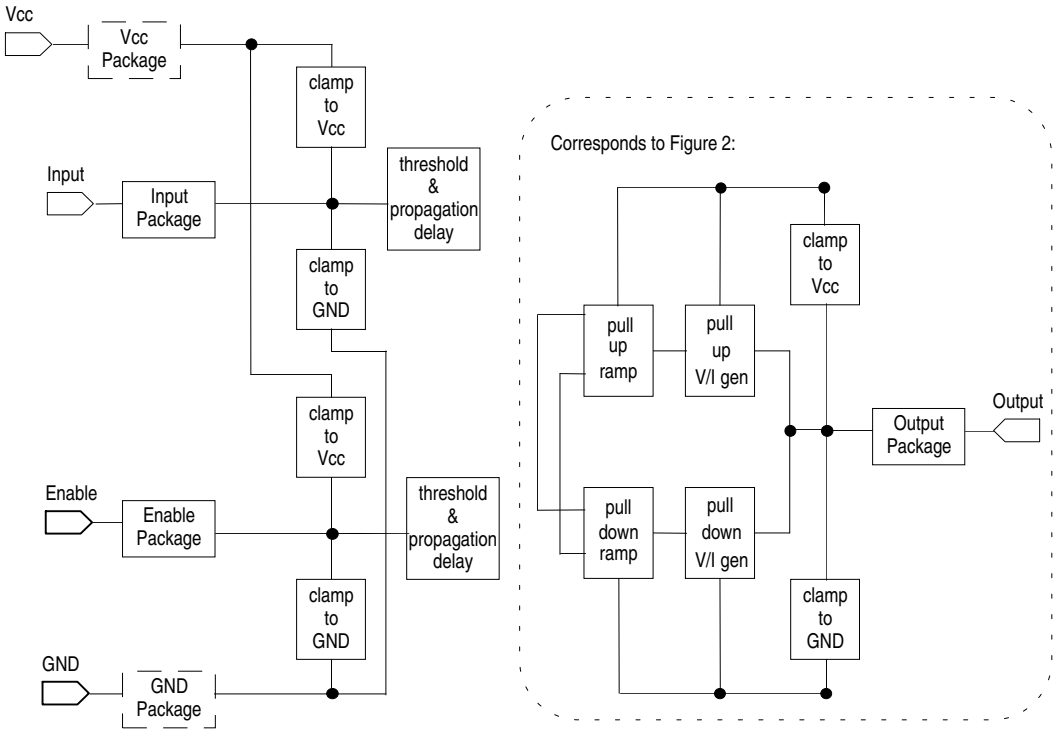


Figure 2: IBIS Behavioral Block Diagram

For hardcopy presentation, a format has been developed that is easier to read than the machine-parsable ASCII format. A page of such tabulated IBIS data is called an information sheet. Figure 3 shows the location of the data for each element on an example information sheet.

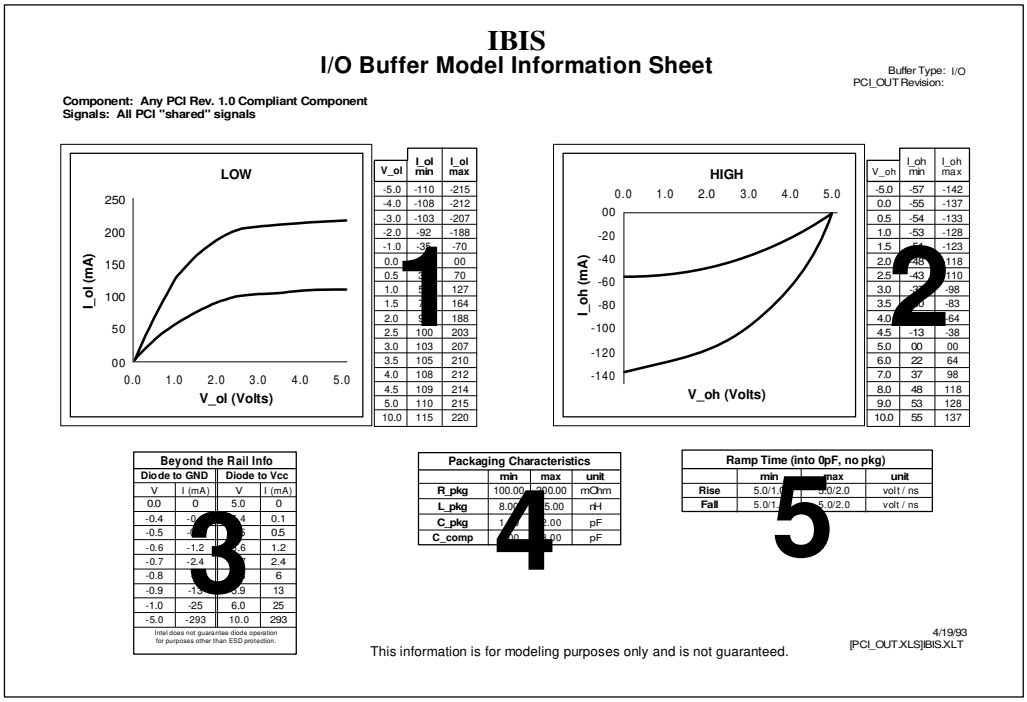


Figure 3: Example I/O Buffer Model Information Sheet

The tabular elements of the information sheet correspond to the keywords in the ASCII format specification:

- Element 1 contains the `Pulldown` information, including the minimum and maximum currents for the given voltages of the pull-down. The table lists voltages from -5V to 10V ($-V_{CC}$ to $2V_{CC}$). The adjacent graph shows the active region (in this case, 0V to 5V) characteristics.

These currents are provided to improve the accuracy of certain simulators. Many simulations benefit from including these characteristics in the model. For simulators that do not extrapolate unspecified voltages, the ranges given are more than adequate.

- Element 2 contains the `Pullup` information, modeling the characteristics of the buffer when driven high.

- Element 3, titled "beyond the rail", contains the `GND_clamp` and `POWER_clamp` information. Diode data, when present, appear in this table. Since some technologies do not include diodes to V_{CC}, this column can be empty.

The `GND_clamp` and `POWER_clamp` diode characteristics are meant to be modeled in parallel with the driver information in elements 1 and 2 (`Pulldown` and `Pullup`), ensuring the diode characteristics are present

even when the output buffer is in tri-state (off). The currents listed in the table can be extremely large and are provided only to allow simulators to construct the proper diode curve.

- Element 5 contains the ramp time for the pull-up and pull-down structures, identified in the specification with the `Ramp` keyword. This information ensures the correct AC operation of the model.

The "min" column represents the longest rise/fall times and the "max" column represents the shortest times. These values often appear very small because they are intrinsic values for the transistors with all packaging and external loads removed. The packaging characteristics are added outside the transistor model (see element #4). *Important: See note under the description of Element 4.*

- Element 4 contains the component and packaging characteristics, identified in the specification with the `Package` keyword. C_comp is the inherent capacitance of the silicon portion of the model (the die, not the package). The package is modeled by the parameters R-L-C_pkg, schematically organized as shown in Figure 1. The table on the information sheets supplies the range (minimum to maximum) for each parameter.

With the information sheet data, interconnect engineers can model the device characteristics for both fast and slow corners. The slow model is useful to determine flight times. The fast model is useful to investigate overshoot, undershoot and crosstalk. Create a slow model by combining the minimum currents (I_ol and I_oh) with the maximum ramp time and the maximum package characteristics. Create a fast model with the largest currents, the fastest ramp, and the minimum package info.

Note: There have been inconsistencies between different IBIS spreadsheets with regard to the way that ramp rates have been treated. If you are using data from an IBIS spreadsheet, make sure that you select the slowest ramp rate (the smallest dV/dT, or the longest ramp time for a given voltage excursion) for use with a slow model and conversely for a fast model. The correct ramp data column will have to be selected by a visual inspection of the data rather than by simply choosing the data in the "max" or "min" columns. Some early IBIS sheets, including the one shown in Figure 4, have interpreted the meaning of min and max in a way that is inconsistent with the IBIS Version 1.1 Specification, which treats "min" as slow. If you are using data from a model file created in conformance to the ASCII IBIS V1.1 Specification, the "min" [Ramp] column for dV/dT_r or ddV/dT_f contains the slow ramp rate data and can be used to generate slow models.

The minimum and maximum data include both temperature and process variations. Voltage variation is normally adjustable within simulation tools, or you can approximate such variation by shifting the V/I data up or down by the desired voltage tolerance.

Input models do not include elements 1, 2, and 4, since no outputs are present. Consequently, the information for inputs normally includes V/I curves for the diodes only, and no ramp times.

Developing IBIS Capability

The following pages describe three circuits software vendors can use to verify their IBIS capability. When a simulator vendor can use IBIS data to create I/O models and correctly simulate all three circuit configurations, that vendor is IBIS capable. Such capability will be announced in advertising and product literature.

To confirm IBIS capability:

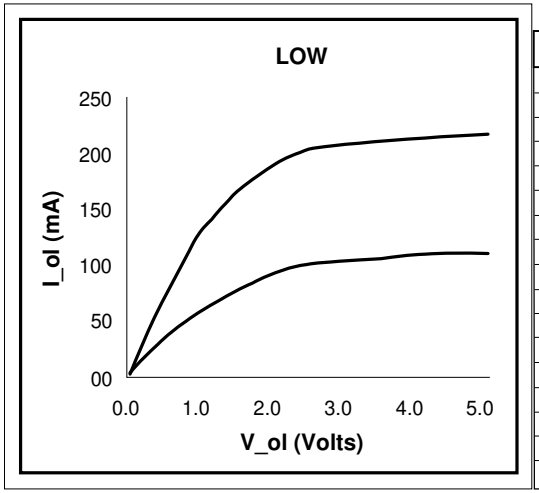
1. Use the IBIS data in Figure 4 to create a PCI_OUT driver model and the IBIS data in Figure 5 to create a PCI_IN receiver model.
2. Simulate the IBIS models under the three circuit configurations described in this section.
3. Compare the results against the specifications and diagrams shown in this section.

IBIS

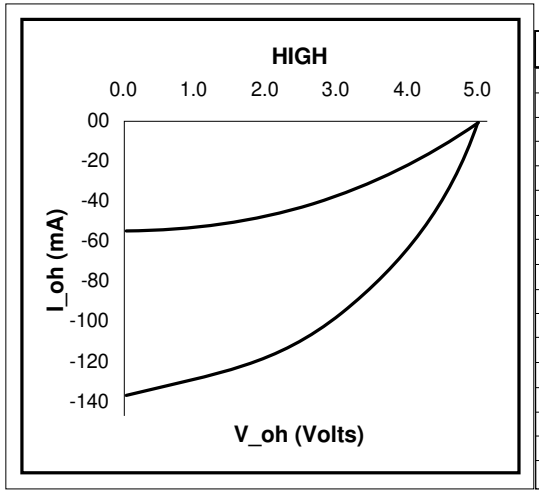
I/O Buffer Information Sheet

Component: Any PCI Rev. 1.0 Compliant Component
Signals: All PCI "shared" signals

Buffer Type:I/O
PCI_OUT Revision:



V_ol	I_ol min	I_ol max
-5.0	-110	-215
-4.0	-108	-212
-3.0	-103	-207
-2.0	-92	-188
-1.0	-35	-70
0.0	00	00
0.5	35	70
1.0	58	127
1.5	76	164
2.0	92	188
2.5	100	203
3.0	103	207
3.5	105	210
4.0	108	212
4.5	109	214
5.0	110	215
10.0	115	220



V_oh	I_oh min	I_oh max
-5.0	-57	-142
0.0	-55	-137
0.5	-54	-133
1.0	-53	-128
1.5	-51	-123
2.0	-48	-118
2.5	-43	-110
3.0	-37	-98
3.5	-30	-83
4.0	-22	-64
4.5	-13	-38
5.0	00	00
6.0	22	64
7.0	37	98
8.0	48	118
9.0	53	128
10.0	55	137

Beyond the Rail Info			
Diode to GND		Diode to Vcc	
V	I (mA)	V	I (mA)
0.0	0	5.0	0
-0.4	-0.1	5.4	0.1
-0.5	-0.5	5.5	0.5
-0.6	-1.2	5.6	1.2
-0.7	-2.4	5.7	2.4
-0.8	-6	5.8	6
-0.9	-13	5.9	13
-1.0	-25	6.0	25
-5.0	-293	10.0	293
Intel does not guarantee diode operation for purposes other than ESD protection.			

Packaging Characteristics			
	min	max	unit
R_pkg	100.00	200.00	mOhm
L_pkg	8.00	15.00	nH
C_pkg	1.00	2.00	pF
C_comp	4.00	8.00	pF

Ramp Time (into 0pF, no pkg)			
	min	max	unit
Rise	5.0/1.0	5.0/2.0	volt / ns
Fall	5.0/1.0	5.0/2.0	volt / ns

Simplified Output Resistance			
	min	max	unit
Low	7.5	19.3	ohms
High	17.1	60.3	ohms
Assumed High Level Low = 5 volts, High = 5 volts			

This information is for modeling purposes only and is not guaranteed.

PCI_OUT Buffer Model

4/19/93
[PCI_OUT.XLS]IBIS.XLT

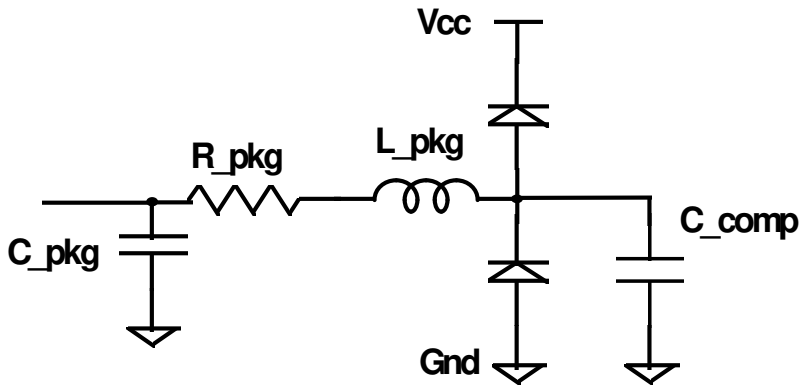
Figure 4: PCI_OUT Information Sheet

IBIS

I/O Buffer Information Sheet

Component: Any PCI Rev. 1.0 Compliant Component
Signals: All PCI 'shared' signals

Buffer Type: I
PCI_IN Provision:



Beyond the Rail Info			
Diode to GND		Diode to Vcc	
V	I (mA)	V	I (mA)
0.0	0	5.0	0
-0.4	-0.1	5.4	0.1
-0.5	-0.5	5.5	0.5
-0.6	-1.2	5.6	1.2
-0.7	-2.4	5.7	2.4
-0.8	-6	5.8	6
-0.9	-13	5.9	13
-1.0	-25	6.0	25
-5.0	-293	10.0	293
Intel does not guarantee diode operation for purposes other than ESD protection			

Packaging Characteristics			
	min	max	unit
R_pkg	100.00	200.00	mOhm
L_pkg	8.00	15.00	nH
C_pkg	1.00	2.00	pF
C_comp	4.00	8.00	pF

intel.

This information is for modeling purposes only and is not guaranteed.

PCI_IN Buffer Model

Figure 5: PCI_IN Information Sheet

Configuration #1

The Configuration #1 circuit is shown in Figure 6. The relevant waveforms are shown in Figures 7 and 8.

Load Type:	simple capacitive load
Circuit Description:	PCI_OUT driver connected to 50 pF capacitor
Simulation:	VCC=5 V, slow buffer, 60 ns period
Waveforms:	1A: 20 ns blow-up of rising edge
	1B: 15 ns blow-up of falling edge
	Plot only the output waveform.

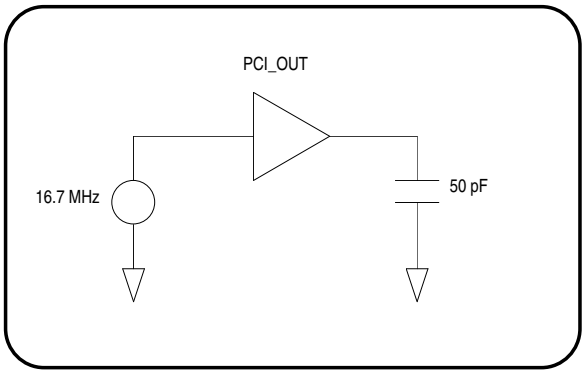


Figure 6: Circuit for Configuration #1

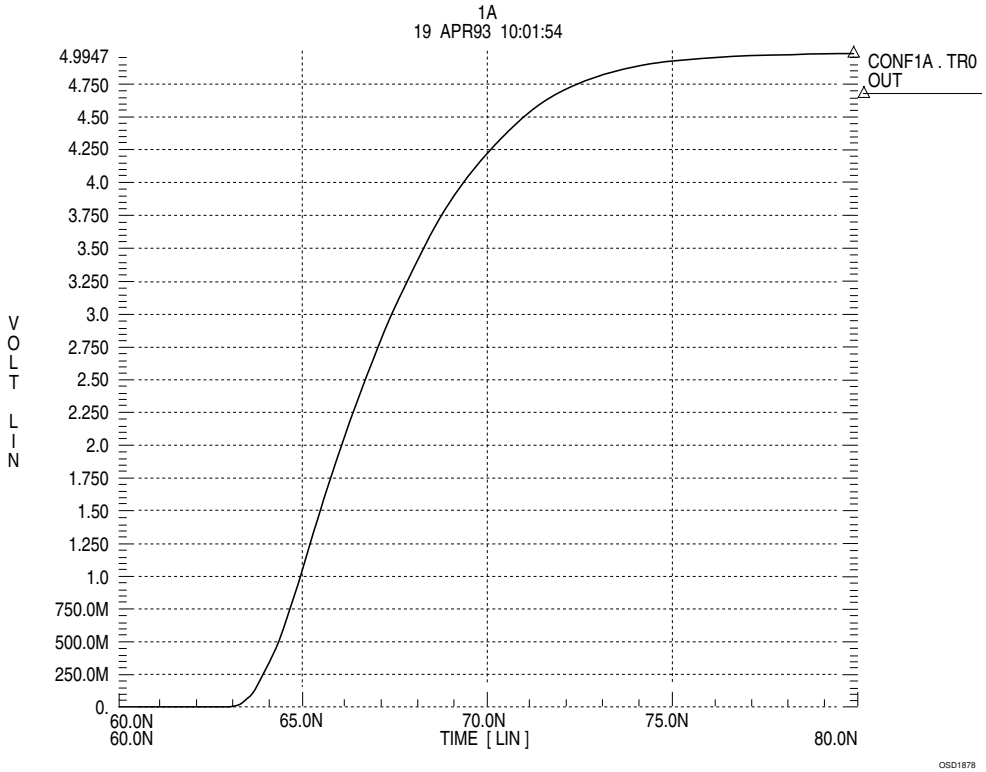


Figure 7: Waveform 1A

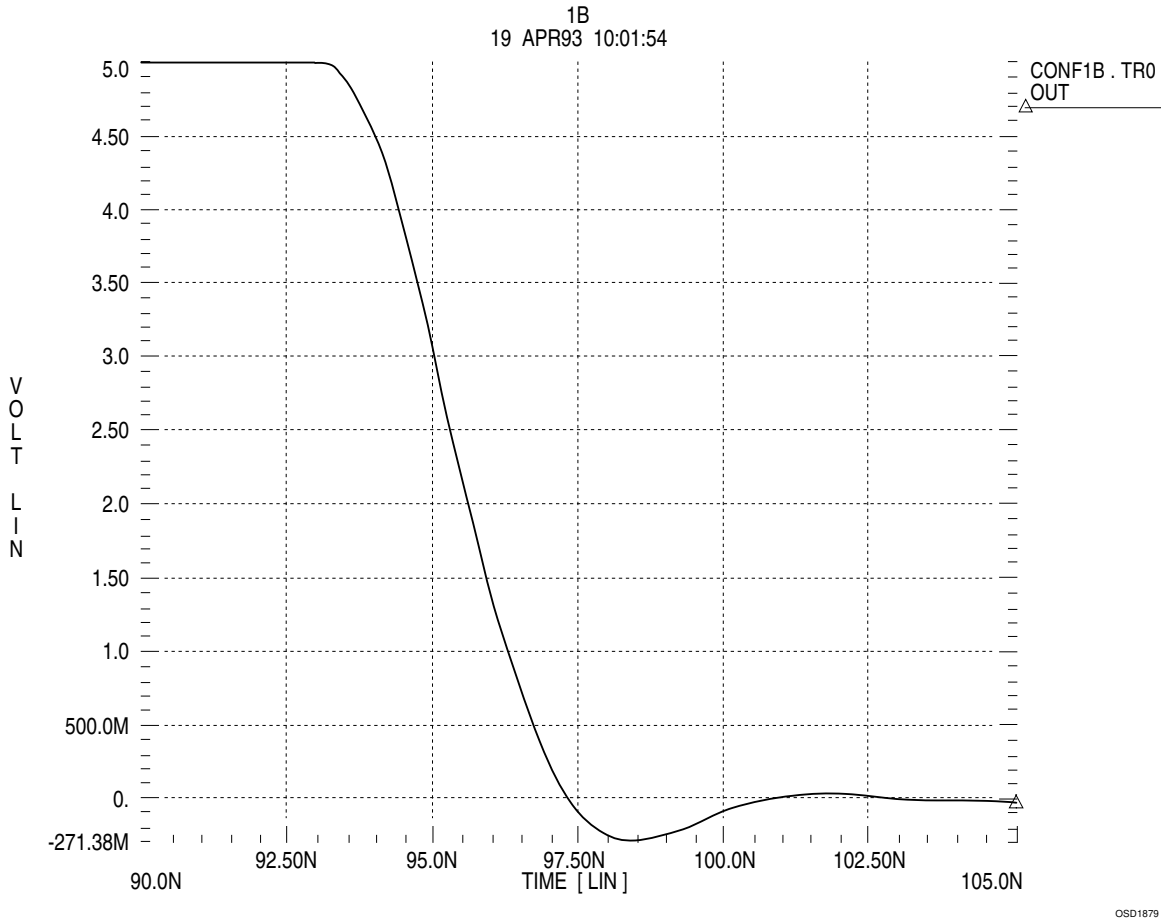


Figure 8: Waveform 1B

Configuration #2

The Configuration #2 circuit is shown in Figure 9. The relevant waveforms are shown in Figures 10 and 11.

Load Type:	simple transmission line load
Circuit Description:	PCI_OUT driver connected to PCI_IN reciever
Simulation:	VCC = 5 V, fast driver, worst-case receiver, 100 ns period
Transmission Line:	Delay = 1.5 ns, Impedance = 65 Ohms, simple Tline is fine
Waveforms:	2A: 20 ns blow-up of rising edge
	2B: 20 ns blow-up of falling edge
	Plot the PCI_OUT output and PCI_IN input (both ends of Tline).

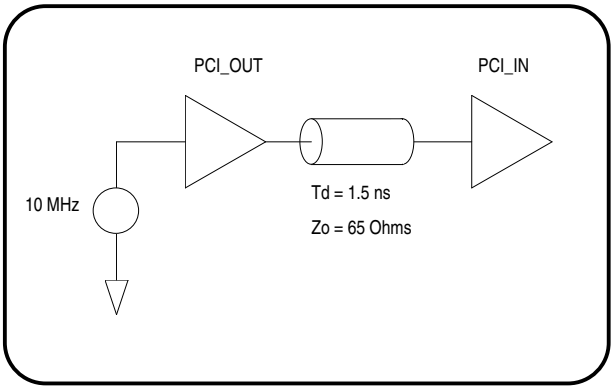


Figure 9: Circuit for Configuration #2

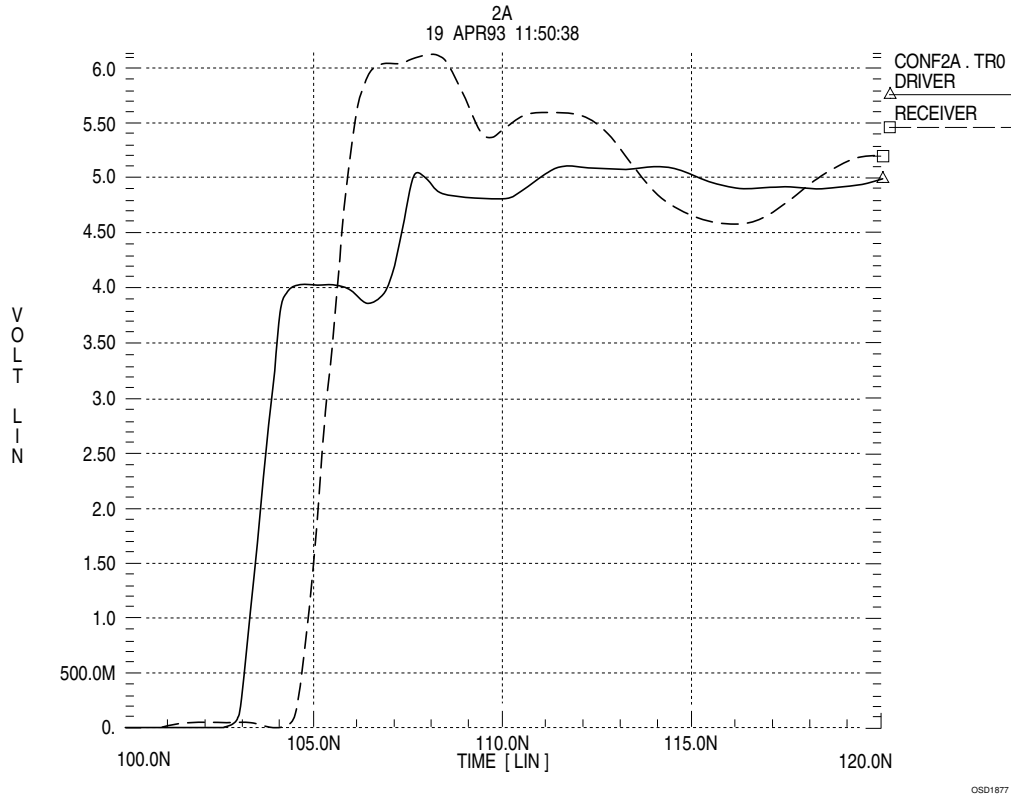


Figure 10: Waveform 2A

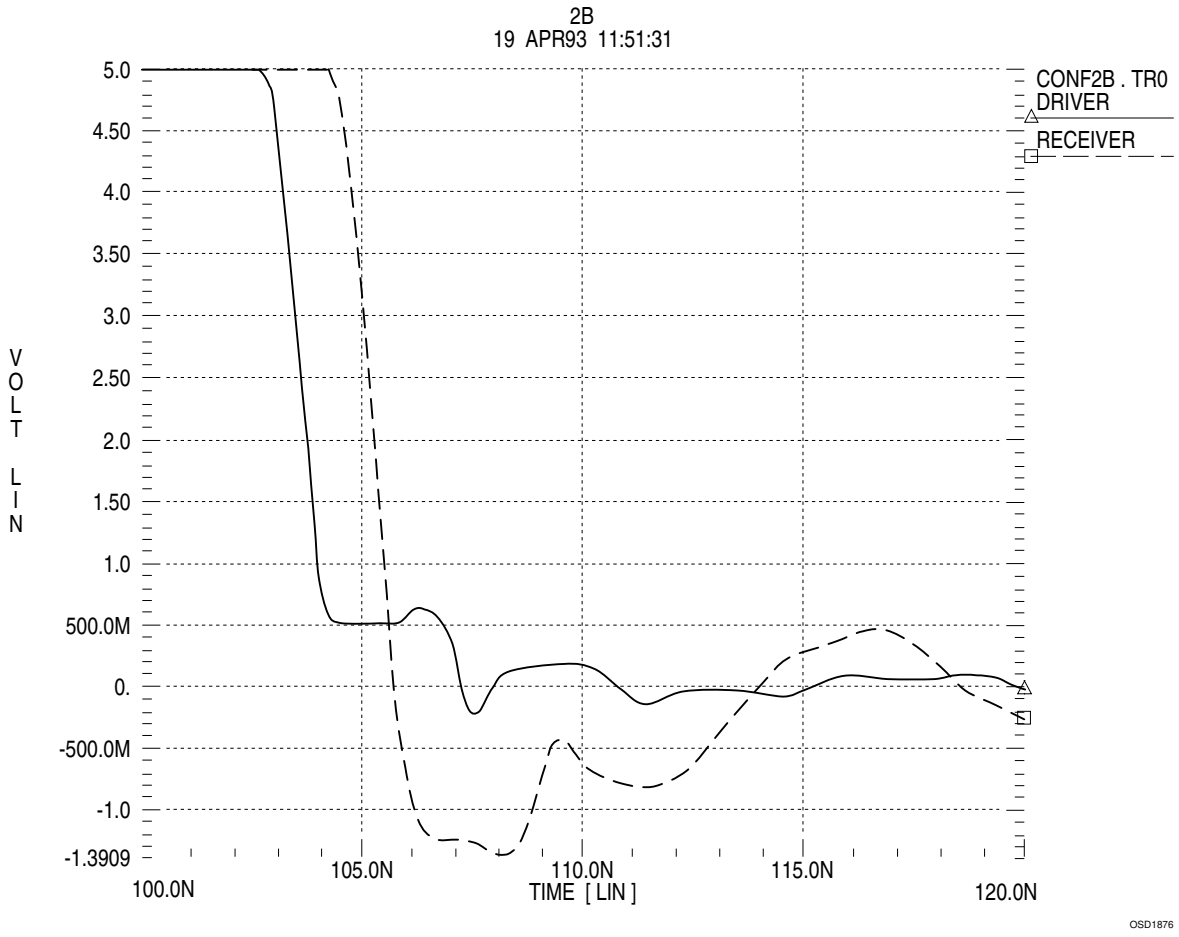


Figure 11: Waveform 2B

Configuration #3

As an additional example, the Configuration #3 circuit is shown in Figure 12. Your IBIS software should be able to handle a circuit of this complexity. Derivation of the relevant waveforms is left as an exercise for the developer.

Load Type:	PCI Speedway, geometric transmission lines
Circuit Description:	PCI_OUT driver connected to nine PCI_IN recievers
Simulation:	worst-case driver, worst-case receiver, 60 nS period
Transmission Line:	Geometric, 6 mil wide, 16 mil or 20 mil to ground plane
Waveforms:	3A: 20 nS blow-up of rising edge, VCC = 4.75 V 3B: 20 nS blow-up of falling edge, VCC = 5.25 V Both plots must show nodes A, B, load2, and load10.

PCB trace (transmission line) segments are:

- 1 inch long for horizontal segments and 1.5 inches long for vertical segments
- 50 ohms characteristic impedance
- 1.8 nS per foot

The dielectric constant is 4.7. Both drivers are PCI_OUT and all receivers are PCI_IN. At all layer changes, you must include 0.5 pF via capacitance.

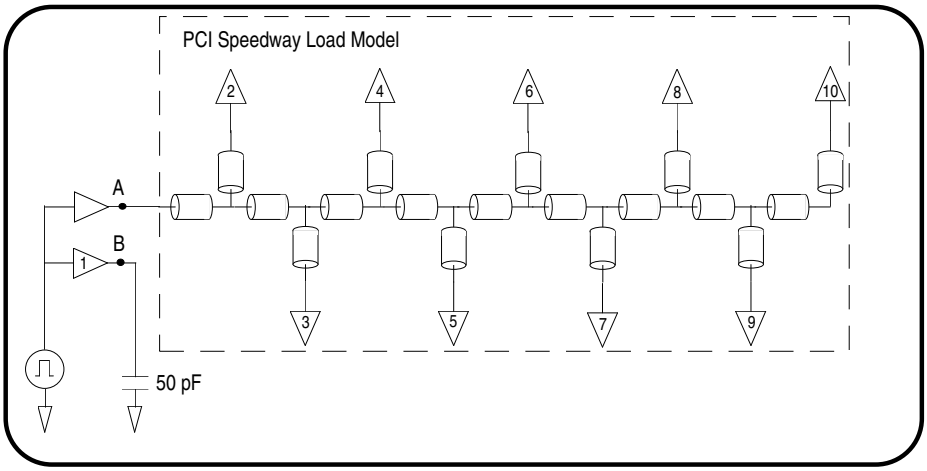


Figure 12: Circuit for Configuration #3

Portion of a Sample .ibs File

```
|*******************************************************************
|
[IBIS Ver]      1.1
[File name]     pcmc.ibs
[File Rev]      2.0
[Date]          6/15/93
[Source]        File originated at Intel Corporation.
[Notes]         The following information corresponds to the A-1
|               stepping of the 82434LX.
[Disclaimer]    This information is for modeling purposes only
|               and is not guaranteed.
|
|*******************************************************************
|
[Component]     82434LX
[Manufacturer]  Intel
[Package]
|               typ             min             max
R_pkg           252m            227m            277m
L_pkg           29.75nH         26.75nH         32.75nH
C_pkg           1.28pF          1.21pF          1.36pF
|
|*******************************************************************
|
[Pin]   signal_name     model_name      R_pin   L_pin   C_pin
|
1       VSS             GND
2       A28             PC040422
3       A24             PC040422

  ......... data deleted for clarity ..............

129     VSS             GND
130     VDD             POWER

  .........  ...................

[Model]         PC040422
Model_type      I/O
Polarity        Non-Inverting
Enable          Active-Low
| Signals       A[0-31]
|                       typ             min             max
C_comp                  5.22pF          2.79pF          7.64pF
|
|*******************************************************************
|
|                       typ             min             max
[Voltage range]         5.0V            4.75V            5.25V
|
|*******************************************************************
|
```

```
[Pulldown]
|       Voltage         I(typ)          I(min)          I(max)
|
    -5.00V         -46.21mA        -35.79mA        -59.83mA
    -4.50V         -45.84mA        -35.48mA        -59.37mA

  .........  ...................

     4.90V          46.14mA         35.73mA         59.74mA
     5.00V          46.21mA         35.79mA         59.83mA
    10.00V          49.95mA         38.87mA         64.35mA
|
[GND_clamp]
|       Voltage         I(typ)          I(min)          I(max)
|
    -5.00V          -1.15A       NA              NA
    -1.10V         -98.50mA      NA              NA
    -1.00V         -71.50mA      NA              NA
  -900.00mV        -46.00mA      NA              NA

  .........  ...................

     0.00V           0.00pA      NA              NA
     5.00V           0.00pA      NA              NA
|
[Pullup]
|       Voltage         I(typ)          I(min)          I(max)
|
    -5.00V          45.06mA         33.33mA         62.10mA
    -4.50V          44.32mA         32.75mA         61.13mA

  .........  ...................

     4.90V         -44.91mA        -33.21mA        -61.90mA
     5.00V         -45.06mA        -33.33mA        -62.10mA
    10.00V         -52.50mA        -40.76mA        -69.53mA
|
[POWER_clamp]
|       Voltage         I(typ)          I(min)          I(max)
|
    -5.00V         442.60mA      NA              NA
    -1.10V          48.70mA      NA              NA
    -1.00V          38.60mA      NA              NA
  -900.00mV         28.50mA      NA              NA

  .........  ...................

  -100.00mV         20.00uA      NA              NA
     0.00V           0.00pA      NA              NA
|
|*****************************************************************************
|
[Ramp]
|                       typ             min             max
dV/dt_r                 1.22/1.22n      0.96/1.51n      1.54/864p
dV/dt_f                 1.33/1.20n      1.07/1.55n      1.64/810p
|
|*****************************************************************************
|
[End]
```

IBIS I/O Buffer Information Specification, Revision 1.1

```
================================================================================
 Statement of Intent:

 In order to enable an industry standard method to electronically transport
 IBIS Modeling Data between silicon vendors, simulation software vendors, and
 end customers, this template is proposed.  The intention of this template is
 to specify a consistent format that can be parsed by software, allowing each
 simulation vendor to derive models compatible with their own product.

 One goal of this template is to represent the current state of IBIS data,
 while allowing a growth path to more complex models / methods (when deemed
 appropriate).  This would be accomplished by a revision of the base
 template, and possibly the addition of new keywords or categories.

 Another goal of this template is to ensure that it is simple enough for
 silicon vendors and customers to use and modify, while ensuring that it is
 rigid enough for software simulation vendors to write reliable parsers.

 Finally, this template is meant to contain a complete description of the I/O
 elements on an entire component.  Consequently, several models will need to
 be defined in each file, as well as a table that equates the appropriate
 buffer to the correct pin and signal name.

 Version 1.1 of this electronic template was finalized by an industry-wide
 group of simulation experts representing various companies and interests.
 "IBIS Open Forum" meetings were held biweekly to accomplish this task.

 Commitment to Backward Compatibility.  Version 1.0 is the first valid IBIS
 ASCII file format.  It represents the minimum amount of I/O buffer
 information required to create an accurate IBIS model of common CMOS and
 bipolar I/O structures.  Future revisions of the ASCII file will add items
 considered to be "enhancements" to Version 1.0 to allow accurate modeling
 of new, or other, I/O buffer structures.  Consequently, all future
 revisions will be considered super sets of Version 1.0, allowing backward
 compatibility.  In addition, as modeling platforms develop support for
 revisions of the IBIS ASCII template, all previous revisions of the
 template must also be supported.

 Version 1.1 update.  The file "ver1_1.ibs" is conceptually the same as
 the 1.0 version of the IBIS ASCII format (ver1_0.ibs).  However, various
 comments have been added for further clarification.

================================================================================

 General syntax rules and guidelines:

 1)  The content of the IBIS_ASCII file is case sensitive, except for file
 names, reserved words and keywords.  Reserved words and keywords are not
 case sensitive, and file names must be all lower case.

 2)  The following words are reserved words and must not be used for
     any other purposes in the document:
        POWER - reserved model name, used with power supply pins,
        GND   - reserved model name, used with ground pins,
        NC    - reserved model name, used with no connect pins,
        NA    - used where data not available.

 3)  File names used in the IBIS_ASCII file must only have lower case
 characters to enhance UNIX compatibility and must conform to DOS rules.
 (The length of a file name should not exceed eight plus three characters
 and it must not contain special characters which are illegal in DOS).
```

4) The IBIS_ASCII file must have no more than 80 characters per line.

5) Anything following the comment character is ignored and considered a comment on that line. The default "|" (pipe) character can be changed by the keyword [Comment char] to any other character. The [Comment char] keyword can be used throughout the file as desired.

6) Keywords must be enclosed in square brackets, [], and must start in column 1 of the line.

7) Valid scaling factors are:
M = mega, k = kilo, m = milli, u = micro, n = nano, p = pico.
When no scaling factors are specified, the appropriate base units are assumed. (These are Volts, Amperes, Ohms, Farads and Henries). The parser will look at only one alphabetic character after a numerical entry, therefore it is enough to use only the prefixes to scale the parameters. However, for clarity, it is allowed to use full abbreviations for the units. (e.g., pF, nH, mA, mOhm). In addition, scientific notation IS allowed (e.g., 1.2345e-12).

8) The V/I data tables should use enough data points around sharply curved areas of the V/I curves to describe the curvature accurately. In linear regions there is no need to define unnecessary data points.

9) Currents are considered positive when their direction is into the component.

Keyword:	[IBIS Ver]
Required:	Yes
Description:	Used to specify the IBIS ASCII template version. This will be used to inform an electronic parser of the kinds of data types that will be present in the file.
Usage Rules:	[IBIS Ver] must be the first keyword in any IBIS file. It is normally on the first line of the file, but can be preceded by comment lines (that must begin with a "|").

[IBIS Ver]	1.1	Used for template variations

Keyword:	[Comment char]
Required:	Optional
Description:	Used to define a new comment character to replace the default "|" (pipe), if desired.
Usage Rules:	The new comment character which is to be defined must be followed by the underscore character and the letters "char". For example: "|_char" redundantly redefines the comment character to be the pipe character. The new comment character will be in effect only following the [Comment char] keyword. The following characters can NOT be used: A B C D E F G H I J K L M N O P Q R S T U V W X Y Z a b c d e f g h i j k l m n o p q r s t u v w x y z 0 1 2 3 4 5 6 7 8 9 [ ] . _ / =
Other Notes:	The [Comment char] keyword can be used throughout the file, as desired.

[Comment char]	|_char

Keyword:	[File name]
Required:	Yes
Description:	Used to specify the name of the IBIS file, "filename.ibs".
Usage Rules:	The file name must comply with normal DOS rules (8 char. max. and no characters that are illegal in DOS). In addition, it must be all lower case, and use the extension ".ibs".

```
[File name]     ver1_1.ibs
|=============================================================================|
|     Keyword:  [File Rev]                                                    |
|    Required:  Yes                                                           |
| Description:  Used to track the revision level of a particular .ibs file.   |
| Usage Rules:  Revision level can be set at the discretion of the engineer   |
|               defining the file.  The following guidelines are recommended: |
|                       0.x     silicon and file in development               |
|                       1.x     pre-silicon file data from silicon model only |
|                       2.x     file correlated to actual silicon measurements|
|                       3.x     mature product, no more changes likely        |
|-----------------------------------------------------------------------------|
[File Rev]      1.0                             | Used for .ibs file variations
|=============================================================================|
|    Keywords:  [Date] [Source] [Notes] [Disclaimer]                          |
|    Required:  Optional                                                      |
| Description:  Optionally used for further file clarifications.              |
| Usage Rules:  The [Date] information is allowed to contain blanks, and be of|
|               any format up to 40 characters.                              |
|-----------------------------------------------------------------------------|
[Date]          04/19/93                        | Latest file revision date
[Source]        Put originator and source of information here.  For example:
                From silicon level SPICE model at Intel,
                From lab measurement at IEI,
                Compiled from manufacturer's data book at Quad Design, etc...
[Notes]         This section can be used for any special notes related
                to the file.
[Disclaimer]    This information is for modeling purposes only, and
                is not guaranteed.              | May vary by component
|=============================================================================|
|     Keyword:  [Component]                                                   |
|    Required:  Yes                                                           |
| Description:  Used to mark the beginning of the IBIS description of the     |
|               integrated circuit named after the keyword.                   |
| Usage Rules:  If the .ibs file contains data for more than one component,   |
|               each section must begin with a new [Component] keyword.  The |
|               length of the Component Name must not exceed 40 characters,  |
|               and blank characters are allowed.                            |
|-----------------------------------------------------------------------------|
[Component]     Component Name
|=============================================================================|
|     Keyword:  [Manufacturer]                                                |
|    Required:  Yes                                                           |
| Description:  Used to clarify the component's manufacturer.                 |
| Usage Rules:  The length of the Manufacturer's Name must not exceed 40      |
|               characters (blank characters are allowed, e.g., Texas         |
|               Instruments).  In addition, each manufacturer must use a      |
|               consistent name in all .ibs files.                            |
|-----------------------------------------------------------------------------|
[Manufacturer]  Manufacturer's Name             | e.g., Intel
|=============================================================================|
|     Keyword:  [Package]                                                     |
|    Required:  Yes                                                           |
| Description:  Used to define a range of values for the default packaging    |
|               resistance, inductance, and capacitance of the component pins.|
| Sub-Params:   R_pkg, L_pkg, C_pkg                                           |
| Usage Rules:  Typical column must be specified.  If data for the other      |
|               columns are not available, they must be noted with "NA".      |
| Other Notes:  If RLC parameters are available for individual pins, they can |
|               be listed in columns 4-6 under keyword [Pin].  The values    |
|               listed in the [Pin] description section override the default |
|               values defined here.                                          |
|-----------------------------------------------------------------------------|
```

```
[Package]
| variable      typ             min             max
R_pkg           250.0m          225.0m          275.0m
L_pkg           15.0nH          12.0nH          18.0nH
C_pkg           18.0pF          15.0pF          20.0pF
|=============================================================================|
|     Keyword:  [Pin]                                                         |
|    Required:  Yes                                                           |
| Description:  Used to associate the component's I/O models to its various   |
|               external pins and signal names.                              |
|  Sub-Params:  signal_name, model_name, R_pin, L_pin, C_pin                  |
| Usage Rules:  All pins on a component must be specified.  The first column  |
|               must contain the pin name.  The second column, signal_name,   |
|               gives the data book name for the signal on that pin.  The     |
|               third column, model_name, associates the I/O model for that   |
|               pin.  Each model_name must have a [Model] keyword below,      |
|               unless it is a reserved model name (POWER, GND, or NC).      |
|                                                                             |
|               Each line must contain either three or six columns.  A pin    |
|               line with three columns only associates the pin's signal and  |
|               model.  Six columns can be used to override the default       |
|               package values (specified under [Package]) FOR THAT PIN ONLY. |
|               When using six columns, the headers R_pin, L_pin, and C_pin   |
|               must be listed.  If "NA" is in columns 4 through 6, the       |
|               default packaging values must be used.                        |
|                                                                             |
|               Column length limits are:                                     |
|                       [Pin]            5 characters max                     |
|                       model_name      20 characters max                     |
|                       signal_name     20 characters max                     |
|                       R_pin            9 characters max                     |
|                       L_pin            9 characters max                     |
|                       C_pin            9 characters max                     |
|-----------------------------------------------------------------------------|
[Pin]   signal_name     model_name      R_pin   L_pin   C_pin
|
  1     RAS0#           Buffer1         200.0m  5.0nH   2.0pF
  2     RAS1#           Buffer2         209.0m  NA      2.5pF
  3     EN1#            Input1          NA      6.3nH   NA
  4     A0              3-state
  5     D0              I/O1
  6     RD#             Input2          310.0m  3.0nH   2.0pF
  7     WR#             Input2
  8     A1              I/O2
  9     D1              I/O2
 10     GND             GND             297.0m  6.7nH   3.4pF
 11     RDY#            Input2
 12     GND             GND             270.0m  5.3nH   4.0pF
|   .
|   .
|   .
 18     VCC3            POWER
 19     NC              NC
 20     Vcc5            POWER           226.0m  NA      1.0pF
|=============================================================================|
|     Keyword:  [Model]                                                       |
|    Required:  Yes                                                           |
| Description:  Used to define a model, and its attributes.                   |
|  Sub-Params:  Model_type, Polarity, Enable, Vinl, Vinh, C_comp              |
| Usage Rules:  Each Input, Output, I/O, 3-state, or Open-drain model must    |
|               begin with the keyword [Model].  The model_name must match    |
|               the one that is listed under the [Pin] keyword and must not   |
|               contain more than 20 characters.  An .ibs file must contain   |
|               enough [Model] keywords to cover all of the model_names       |
|               specified under the [Pin] keyword, except for those          |
|               model_names which use reserved words (POWER, GND and NC).     |
|               Model_names with reserved words are an exception and          |
|               they do not have to have a corresponding [Model] keyword.     |
|               C_comp is allowed to use "NA" for the min and max values only.|
| Other Notes:  A complete [Model] description normally contains the following|
|               keywords:  [Voltage range], [Pullup], [Pulldown], [GND_clamp],|
|               [POWER_clamp], and [Ramp].  However, some models may have only|
|               a subset these keywords.  For example, an input structure    |
|               normally only needs the [Voltage range], [GND_clamp], and    |
|               possibly the [POWER_clamp] keywords.                          |
|               Note that C_comp defines the silicon die capacitance.  This   |
|               value should not include the capacitance of the package.     |
|                                                                             |
|-----------------------------------------------------------------------------|
[Model]         model_name
```

```
Model_type      Input, Output, I/O, 3-state, Open_drain | List one only
Polarity        Non-Inverting, Inverting                | List one only, if any
Enable          Active-High, Active-Low                 | List one only, if any
| Signals       RAS, CAS, A(0-64), D(0-128),...         | Local list, if desired
Vinl = 0.8V                                | input logic "low" DC voltage, if any
Vinh = 2.0V                                | input logic "high" DC voltage, if any
| variable      typ             min             max
C_comp          12.0pF          10.0pF          15.0pF
|================================================================================|
|     Keyword:  [Voltage range]                                                  |
|    Required:  Yes                                                              |
| Description:  Used to define the power supply voltage tolerance over which     |
|               the model is intended to operate.                                |
| Usage Rules:  Actual voltages (not percentages) are to be presented in the     |
|               usual typ, min, max format.  "NA" is allowed for the min and     |
|               values only.                                                     |
| Other Notes:  [Voltage range] also describes the voltage range over which      |
|               the various V/I curves and ramp rates were derived.              |
|--------------------------------------------------------------------------------|
| variable              typ             min             max
[Voltage range]         5.0V            4.5V            5.5V
|================================================================================|
|    Keywords:  [Pulldown], [Pullup], [GND_clamp], [POWER_clamp]                 |
|    Required:  Yes, if they exist in the device                                 |
| Description:  The data points under these keywords define the V/I curves of    |
|               the pulldown and pullup structures of an output buffer and the  |
|               V/I curves of the clamping diodes connected to the GND and the  |
|               POWER pins, respectively.                                        |
| Usage Rules:  In each of these sections the first column contains the          |
|               voltage value, and the three remaining columns hold the         |
|               typical, minimum, and maximum current values.   The four        |
|               entries, Voltage, I(typ), I(min), and I(max) must be placed on  |
|               a single line and must be separated by at least one white       |
|               space or tab character.                                         |
|               All four columns are required under these keywords, however     |
|               data is only required in the typical column.  If minimum        |
|               and/or maximum current values are not available, the reserved    |
|               word "NA" must be used.  "NA" can be used for currents in the    |
|               typical column, but numeric values MUST be specified for the    |
|               first and last voltage points on any V/I curve.  Each V/I       |
|               curve must have at least 2, but not more than 100, voltage      |
|               points.                                                         |
| Other Notes:  It should be noted that the V/I curve of the [Pullup] and the    |
|               [POWER_clamp] structures are 'Vcc relative', meaning that the   |
|               voltage values are referenced to the Vcc pin.  The voltages in  |
|               the data tables are derived from the equation:                   |
|                       Vtable = Vcc - Voutput                                   |
|               Therefore, for a 5V component, -5 V in the table actually       |
|               means 5 V above Vcc, which is +10 V with respect to ground;     |
|               and 10 V means 10 V below Vcc, which is -5 V with respect to    |
|               ground.  Vcc-relative data is necessary to model a pullup       |
|               structure properly, since the output current of a pullup        |
|               structure depends on the voltage between the output and Vcc     |
|               pins and not the voltage between the output and ground pins.    |
|               Note that the [GND_clamp] V/I curve can include quiescent       |
|               input currents, or the currents of a 3-stated output if so      |
|               desired.                                                         |
|--------------------------------------------------------------------------------|
[Pulldown]
|  Voltage   I(typ)    I(min)    I(max)
|
   -5.0V    -40.0m    -34.0m    -45.0m
   -4.0V    -39.0m    -33.0m    -43.0m
|    .
|    .
    0.0V      0.0m      0.0m      0.0m
|    .
|    .
    5.0V     40.0m     34.0m     45.0m
   10.0V     45.0m     40.0m     49.0m
|
[Pullup]
|
|  Voltage   I(typ)    I(min)    I(max)
|
   -5.0V     32.0m     30.0m     35.0m
   -4.0V     31.0m     29.0m     33.0m
|    .
|    .
    0.0V      0.0m      0.0m      0.0m
```

```
|    .
|    .
    5.0V    -32.0m    -30.0m    -35.0m
   10.0V    -38.0m    -35.0m    -40.0m
|
[GND_clamp]
|
|  Voltage   I(typ)    I(min)    I(max)
|
   -5.0V  -3900.0m  -3800.0m  -4000.0m
   -0.7V    -80.0m    -75.0m    -85.0m
   -0.6V    -22.0m    -20.0m    -25.0m
   -0.5V     -2.4m     -2.0m     -2.9m
   -0.4V      0.0m      0.0m      0.0m
    5.0V      0.0m      0.0m      0.0m
|
[POWER_clamp]
|
|  Voltage   I(typ)    I(min)    I(max)
|
   -5.0V   4450.0m       NA        NA
   -0.7V     95.0m       NA        NA
   -0.6V     23.0m       NA        NA
   -0.5V      2.4m       NA        NA
   -0.4V      0.0m       NA        NA
    0.0V      0.0m       NA        NA
|=============================================================================|
|     Keyword:  [Ramp]                                                        |
|    Required:  Yes, except for inputs                                        |
| Description:  Used to define the rise and fall times of a buffer.           |
|  Sub-Params:  dV/dt_r, dV/dt_f                                              |
| Usage Rules:  These parameters describe an ideal slope and can be expressed |
|               as a ratio of any reasonable voltage and time values as shown |
|               in the examples.  The [Ramp] values are allowed to use "NA"   |
|               for the min and max values only.                              |
|-----------------------------------------------------------------------------|
[Ramp]
| variable      typ             min             max
dV/dt_r         4.2/1.8n        3.5/2.5n        5.0/1.1n
dV/dt_f         2.5/1.5n        2.0/2.3n        3.0/0.8n
|=============================================================================|
|     Keyword:  [End]                                                         |
|    Required:  Yes                                                           |
| Description:  Used to define the end of the .ibs file.                      |
|-----------------------------------------------------------------------------|
[End]
|=============================================================================|
|                        NOTES ON DATA DERIVATION METHOD                      |
|                                                                             |
| This section explains how data values are derived.  The intention here is to |
| avoid over-guardbanding, enabling simulation results that are meaningful and |
| useful.  This is accomplished by having each silicon vendor base their data |
| on typical process data, and then derate by voltage and temperature, and a  |
| proprietary "X%" factor.  This methodology also has the nice feature that   |
| the data can be derived either from vendor-proprietary silicon models, or   |
| typical device measurement over temperature/voltage.                        |
|                                                                             |
| 1) V/I curves for CMOS devices:                                             |
|       typ = nominal voltage,  50 degrees C, typical process                |
|       min = low voltage tol, 100 degrees C, typical process, minus "X%"     |
|       max = hi voltage tol,    0 degrees C, typical process, plus  "X%"     |
|                                                                             |
|    V/I curves for bipolar devices:                                          |
|       typ = nominal voltage,  50 degrees C, typical process                |
|       min = low voltage tol,   0 degrees C, typical process, minus "X%"     |
|       max = hi voltage tol,  100 degrees C, typical process, plus  "X%"     |
|                                                                             |
|       where X% should be statistically determined by the silicon vendor     |
|       based on numerous fab lots, test chips, process controls, ...  The    |
|       value of X need not be published in the IBIS file, and may decrease   |
|       over time as data on the I/O buffers and silicon process increases.   |
|       Temperatures are junction temperatures.                               |
|                                                                             |
| 2) Voltage Ranges:                                                          |
|       Points for each curve must span the voltages listed below:            |
|                                                                             |
|       Curve                   Low Voltage             High Voltage          |
|       -----------             -----------             ------------          |
|       [Pulldown]              GND - POWER             POWER + POWER         |
|       [Pullup]                GND - POWER             POWER + POWER         |
```

```
       [GND_clamp]             GND - POWER             GND + POWER
       [POWER_clamp]           POWER                   POWER + POWER

       For example, a device with a 5 V power supply voltage should be
       characterized between (0 - 5) = -5 V and (5 + 5) = 10 V;
       and a device with a 3.3 V power supply should be characterized
       between (0 - 3.3) = -3.3 V and (3.3 + 3.3) = 6.6 V for the
       pulldown curve.

 3) Ramp Rates:
       The ramp rates (listed in AC characteristics below) should be
       derived by:
       1.  Start with silicon model, remove all packaging.
       2.  Attach 50 Ohm resistor to GND to derive rising edge ramp.
       3.  Attach 50 Ohm resistor to POWER to derive falling edge ramp.
       4.  Due to the resistor, output swings will not make a full
           transition as expected.  However the pertinent data can still
           be collected as follows:
              a)  determine the 20% to 80% voltages of the 50 Ohm swing
              b)  measure this voltage change as "dv"
              c)  measure the amount of time required to make this swing "dt"
       5.  Post the value as a ratio "dv/dt", the simulation tool vendor
           will extrapolate this value to span the required voltage swing
           range in the final model.
       6.  Typ, Min, and Max must all be posted, and are derived at the
           same extremes as the V/I curves, which are:

       Ramp times for CMOS devices:
           typ = nominal voltage,  50 degrees C, typical process
           min = low voltage tol, 100 degrees C, typical process, minus "Y%"
           max = hi voltage tol,    0 degrees C, typical process, plus  "Y%"

       Ramp times for bipolar devices:
           To be determined by manufacturer.

           Note that the derate factor, "Y%", may be different than that used
           for the V/I curve data.  This factor is similar to the X% factor
           described above.  As in the case of V/I curves, temperatures are
           junction temperatures here also.

       7.  The rise time of an open-drain device must be measured into
           a 50 Ohm pullup resistor tied to the power pin.

 It is expected that this data will be created from silicon vendor
 proprietary silicon-level models, and later correlated with actual device
 measurement.
================================================================================
```