

IBIS Open Forum Minutes

Meeting Date: **November 22, 2013**
Meeting Location: **Yokohama, Japan**

VOTING MEMBERS AND 2013 PARTICIPANTS

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ZTE Corporation	Huifeng Chen, Fengling Gao, Tao Guo, Hui Jiang, Zhi Zhou, Shunlin Zhu

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Meeting Number	Meeting Password
December 6, 2013	205 475 958	IBIS

For teleconference dial-in information, use the password at the following website:

<https://ciscosales.webex.com/ciscosales/j.php?J=205475958>

All teleconference meetings are 8:00 AM to 9:55 AM US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting. When calling into the meeting, follow the prompts to enter the meeting ID. For new, local international dial-in numbers, please reference the bridge numbers provided by Cisco Systems at the following link:

http://www.cisco.com/web/about/doing_business/conferencing/index.html

NOTE: "AR" = Action Required.

WELCOME AND KEYNOTE COMMENTS

The IBIS Open Forum summit was held in Yokohama, Japan, co-located with the Electronics Design Solutions Fair (EDS Fair) at the Pacifico Yokohama Conference Center. About 107 people representing 74 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

<http://www.eda.org/pub/ibis/summits/nov13c/>

Michael Mirmak opened the eighth Asian IBIS Summit in Yokohama, Japan. Haruhiro Saito (JEITA EC Working Group Chair and Sony Corporation) welcomed everyone and looked forward to a productive meeting. Yoshinori Fukuba (JEITA LPB Working Group Chair and Toshiba) also provided introductions and welcomes and mentioned ongoing LPB work with IEEE. Michael provided some brief remarks, thanked JEITA for their support and providing excellent facilities.

INTRODUCING IBIS 6.0

Michael Mirmak (Intel Corporation, USA)

Michael Mirmak noted that IBIS 6.0 was released September 20, 2013. Major additions focus on IBIS-AMI including added support for redrivers and retimers and IBIS-ISS and Touchstone. The document is now easier to read and use. Michael gave detailed examples of modeling a mid-bus repeater. In IBIS 6.0, IBIS-ISS can be used to represent the complex analog buffer behavior of an AMI model. Multiple files in different locations are now supported for AMI models. Use of IBIS 6.0 improved analog modeling can help ensure model portability. Among issues to resolve is improving IBIS package modeling. Package modeling formats are being discussed with a target to include an update in the next major IBIS release. Developing an IBISCHK6 syntax parser is a focus now.

A question was asked about whether major and minor versions will be released twice a year. Michael responded that it depends. He expects the audience to provide feedback on IBIS feature needs and schedule.

IBIS SUMMARY DOCUMENTS

Bob Ross (Teraspeed Consulting Group, USA)
[Presented by Anders Ekholm (Ericsson, Sweden)]

Anders Ekholm presented information about several documents created by Bob Ross to accompany the IBIS 6.0 specification release. IBIS 6.0 contains a keyword hierarchy tree in section 3.1. Bob updated an unofficial hierarchy document from 2007 with information from IBIS versions 5.1 and 6.0. Extra information in this document includes when items were added at major versions. Bob also created an unofficial evolution document featuring updated columns showing major version evolution, rules and changes evolution and significant subparameter selections such as the *_type subparameter choices.

Anders also noted that Bob helped create four new summary tables in section 10.7 of the IBIS 6.0 specification. These tables include Usages, Types and Formats for Reserved Parameters and Types for Format values. The summary information provides quick references for IBIS and IBIS-AMI syntax. The documents are found on the IBIS website along with the IBIS 6.0 specification.

IBIS AMI MODEL (ALGORITHMIC MODEL INTERFACE) – THEORY & STRUCTURE

Shinichi Maeda (KEI Systems, Japan)

Maeda-san began by summarizing the types of SerDes interfaces that require IBIS-AMI models. He then described the theory behind statistical simulations, including the LTI system assumptions. He defined the differences between traditional IBIS models and IBIS-AMI models and gave details on AMI model syntax. He then presented an IBIS-AMI reference flow. He concluded with some concerns for IBIS-AMI including inability to check the model accuracy, simulator dependencies and minimal documentation.

Someone commented that the claims on lack of interoperability with tool dependent models were mostly an IBIS 5.0 problem. Another comment was about a typo of 'AMI' on slide 16. Another comment was that the syntax on slide 17 showed a very sharp edge rate ramp. A survey of people in the room showed that only a few have used IBIS-AMI.

CORRELATION BETWEEN IBIS5.X AND SPICE

Kazuki Murata (Ricoh Company Ltd., Japan)

Murata-san performed two correlation studies using IBIS models and Spice models. The first study compared an IBIS-AMI model of a Ricoh SerDes Tx with Spice and lab measurements. Simulations were performed with four different tools. Murata-san concluded that the IBIS-AMI model was highly correlative with Spice and measurements, differences between simulators were not recognized and simulation time was much shorter than typical transient simulation time.

Murata-san then showed the results of a correlation study comparing an IBIS 5.1 power-aware model to Spice. He simulated a DDR3 system with 70 I/Os to show SSO conditions. ISSO and Composite Current keywords were used. Simulating the system using Spice models took 24 hours. The IBIS 5.1 power-aware models were used in two simulators. At 533 MHz, one simulator appeared to have low accuracy due to overclocking issues. He also showed that SSO noise correlated better with Spice when a voltage controlled capacitor was used to model the on-die power supply decoupling. Murata-san noted that jitter due to SSO was smaller using the IBIS models than in Spice.

AN ADVANCED BEHAVIORAL BUFFER MODEL WITH OVER-CLOCKING SOLUTION

Yingxin Sun and Raymond Y. Chen (Cadence Design Systems, USA)

[Presented by Morihiro Nakazato (Cadence Design Systems, Japan)]

Morihiro Nakazato began by describing the mechanisms related to overclocking of IBIS models. A simulator that does not properly window V-T data will give incorrect results, sometimes showing missing bits. V-T windowing works well for IBIS 4.2 models. However, for IBIS 5.0 models that include I-T data, using the same V-T windowing algorithm will cut off the pre-driver current seen in the composite current I-T data. Nakazato-san proposed an advanced over-clocking solution, where a pre-driver stage was added to the driver stage. With this model, the composite current could be broken into two portions, the contribution from the driver and the contribution from the pre-driver. The proposed over-clocking solution could be implemented into an advanced IBIS simulator to automatically handle the windowing of both V-T and I-T data. With this solution, very good correlation was seen between IBIS and the original transistor model for real SSO simulation, even under over-clocking scenarios.

Michael Mirmak asked if we were to accomplish this in the specification, we would need a new keyword for pre-driver Composite Current, correct? Nakazato-san responded that yes, that would be one solution for the next IBIS version.

COMBINED I-V TABLE CHECKING PROBLEM

Bob Ross*, Yingxin Sun** and Joy Li** (*Teraspeed Consulting Group, **Cadence Design Systems, USA)

[Presented by Anders Ekholm (Ericsson, Sweden)]

Anders Ekholm began by describing BUG140, where unexpected non-monotonic warnings are issued for combined I-V tables. There is no specification requirement that individual or combined I-V tables be monotonic. Combined table checks were added to the IBIS parser following BUG94. Non-monotonicity often occurs outside of normal simulation regions (clamp regions) and is not a problem for simulation software. Anders walked through a simple example to demonstrate how piecewise linear interpolation methods can cause non-monotonicities when combining two data sets. Anders then showed two test case examples from BUG140. The Quality task group discussed several options for fixes including using more complicated SPLINE fitting algorithms. The final resolution was to change the warning to a note.

IBIS MODEL FOR IO-SSO ANALYSIS

Thunder Lay and Jack W.C. Lin (Cadence Design Systems, Taiwan)

[Presented by Takuya Moriya (Cadence Design Systems, Japan)]

Takuya Moriya began by defining Simultaneous Switching outputs Noise (SSN). SSN impacts timing and noise margin and becomes a bigger problem as voltages decrease and data rates increase. Traditional SSN simulations can be pessimistic when the analysis excludes an on-die decoupling model or includes an estimated on-die decoupling model. An accurate RC or distributed chip PDN model is needed for realistic power/ground noise analysis. Moriya-san showed a method of using [External Circuit] in IBIS 5.1 to incorporate on-die and package models into the buffer. Moriya-san then showed a case study of a DDR data byte lane including a power-aware IBIS model, on-chip decoupling model and PCB and package S-parameters converted to broadband-Spice models. Without a chip PDN model, SSN is overestimated. With an on-die RC PDN model, the noise is underestimated. Using a distributed broadband model of the on-die PDN gave the most realistic results. Moriya-san summarized that for tighter timing and noise budgets in LPDDR3 or DDR4, system level SSN analysis is helpful for design margin assessment.

IBIS MODEL WHICH IS ACCESSIBLE TO BEGINNERS

Kazuhiko Kusunoki (Wadow, Japan)

Kusunoki-san began by thanking a senior IBIS simulation expert present in the audience who has been in the simulation world for 30 years. He went on to give an overview of the types of products being designed in Japan. The majority of Wadow's projects are using existing technology, not leading edge concepts. Product issues therefore tend to be focused not on GHz+ frequency issues but on reducing PCB layer counts while increasing clock frequencies and decreasing EMI issues. He noted that the number of IBIS model beginners is increasing

daily, as most products have some SI issues. However, budget and time constraints are not encouraging users to learn IBIS in-depth. Kusunoki-san called for IBIS users to join a Facebook group called "CROSSTALKS" which discusses IBIS issues.

CONCLUDING ITEMS

Michael Mirmak thanked the attendees and co-sponsors and JEITA for sponsoring and arranging the meeting. The meeting adjourned at approximately 5:30 PM.

NEXT MEETING

The next IBIS Open Forum teleconference will be held December 6, 2012 from 8:00 to 10:00 AM US Pacific Time.

NOTES

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This meeting was conducted in accordance with ANSI guidance.

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State your request.

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To obtain general information about IBIS, to ask specific questions for individual response, and to inquire about joining the IBIS Open Forum as a full Member.

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To send a message to the IBIS Users' Group Reflector. This is used mostly for IBIS clarification, current modeling issues, and general user concerns. Job posting information is not permitted.

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To report ibischk parser BUGs as well as tschk2 parser BUGs. The BUG Report Form for ibischk resides along with reported BUGs at:

<http://www.eda.org/ibis/bugs/ibischk/>
<http://www.eda.org/ibis/bugs/ibischk/bugform.txt>

The BUG Report Form for tschk2 resides along with reported BUGs at:

http://www.eda.org/ibis/tschk_bugs/
http://www.eda.org/ibis/tschk_bugs/bugform.txt

icm-bug@eda.org

To report icmchk1 parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda.org/ibis/icm_bugs/
http://www.eda.org/ibis/icm_bugs/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

<http://www.eda.org/ibis/bugs/s2ibis/bugs2i.txt>
<http://www.eda.org/ibis/bugs/s2ibis2/bugs2i2.txt>
<http://www.eda.org/ibis/bugs/s2iplt/bugsplt.txt>

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

<http://www.eda.org/ibis>

Check the IBIS file directory on eda.org for more information on previous discussions and results:

<http://www.eda.org/ibis/directory.html>

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IBIS – SAE STANDARDS BALLOT VOTING STATUS

I/O Buffer Information Specification Committee (IBIS)

Organization	Interest Category	Standards Ballot Voting Status				
		November 1, 2013	November 15, 2013	November 19, 2013	November 22, 2013	
Agilent Technologies	User	Active	X	X	X	X
Altera	Producer	Inactive	X	-	-	-
ANSYS	User	Active	-	X	X	X
Applied Simulation Technology	User	Inactive	-	-	-	-
Cadence Design Systems	User	Active	X	X	X	X
Ericsson	Producer	Active	-	X	X	X
Foxconn Technology Group	Producer	Inactive	-	-	X	-
Huawei Technologies	Producer	Inactive	-	X	-	-
IBM	Producer	Inactive	X	-	-	-
Infineon Technologies AG	Producer	Inactive	-	-	-	-
Intel Corp.	Producer	Active	X	X	X	X
IO Methodology	User	Active	-	X	X	-
LSI	Producer	Inactive	X	-	-	-
Maxim Integrated Products	Producer	Inactive	-	-	-	-
Mentor Graphics	User	Inactive	X	-	-	-
Micron Technology	Producer	Inactive	X	-	-	-
Signal Integrity Software	User	Inactive	X	-	-	-
Synopsys	User	Inactive	-	X	-	-
Teraspeed Consulting	General Interest	Inactive	X	-	-	-
Toshiba	Producer	Inactive	-	-	-	X
Xilinx	Producer	Inactive	-	-	-	-
Zuken	User	Inactive	-	-	-	X

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- MUST ATTEND TWO CONSECUTIVE MEETINGS TO ESTABLISH VOTING MEMBERSHIP
- MEMBERSHIP DUES CURRENT
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