For more information contact:

IBIS Open Forum
Will Hobbs, (503) 696-4369
Jon Powell, (805) 988-8250

For Immediate Release

IBIS Signal Integrity Model Specification Announced

Emerging Standard Supports Early, Accurate Models for Signal Integrity Simulations of High-speed Digital Systems

BEAVERTON, Ore. — Oct. 12, 1993 — A group of Electronic Design Automation (EDA) and semiconductor companies today announced the development and adoption of Version 1.1 of the I/O Buffer Information Specification (IBIS) standard for integrity models. This emerging standard promises to deliver models earlier, and provide superior simulation performance and accuracy than has been possible using traditional signal integrity model development approaches. As digital system design engineers are increasingly challenged by higher clock speeds and special packaging, signal integrity simulation is becoming imperative. IBIS addresses one of the fundamental simulation issues, that of model availability.

IBIS Standard Provides Early Models While Protecting Proprietary Information

IBIS is a consistent format that semiconductor vendors can use to specify the analog characteristics of input and output buffers. This essential information is readily transformed into accurate models by end users and simulation tool vendors. The resulting behavioral models allow users to perform high-speed, accurate signal-integrity simulations of their digital system interconnects.

Most existing I/O buffer model development methodologies are based on actual circuit designs. Such descriptions reveal detailed information not only about the buffer design, but also about the underlying, proprietary fabrication processes. In contrast, IBIS uses voltage-versus-current characteristics, along with additional circuit, package and timing information to describe

the buffers. This form of data protects the semiconductor vendor's proprietary information about the design, and process technology while still providing a highly useful and accurate model for the end users.

"By standardizing on a non-proprietary method of specifying models, the industry has a win-win situation," states Jon Powell, product manager, transmission line tools at Quad Design. "Semiconductor companies can deliver the information once, EDA tools have a ready and easy source for models, and end users gain high-performance, accurate models."

Behavioral IBIS Models Are Easy to Generate and Offer Superior Performance

The data used to develop an IBIS model can be easily derived from simulations of the actual circuits or measured directly using commonly available laboratory equipment. This easily derivable data includes V-I curves for high- and low-output transitions; V-I curves for clamp diodes; high/low ramp times; component capacitance; and per-pin package resistance, inductance and capacitance. By simplifying the data collection and removing proprietary issues, the semiconductor vendors can provide IBIS models prior to, or at the same time as, the availability of first components.

Because IBIS models are behavioral, simulations run much faster than corresponding structural models. Speed improvements of 25 times are not uncommon. IBIS accomplishes this performance improvement without sacrificing accuracy by incorporating the specification of many non-linear effects of the I/O design, including package parasitics and forward-biased ESD protection diode effects.

"We have the opportunity to break open the logjam in model availability for signal integrity analysis by creating accurate, efficient models that can be delivered with the silicon," says Shiv Tasker, vice president and general manager, systems physical design group at Cadence Design Systems. "The availability of these models will have a major impact on how quickly new parts introduced by IC vendors will be designed into new products. It is therefore in the customers', and IC and EDA vendors' interest to actively encourage adoption of such critical standards as IBIS."

First Models Available

Intel and IBIS development group have been working regularly over the last year to refine the specification, benchmark the resulting models, and verify the simulations from the models against laboratory measurements of actual circuits. Intel has developed and released the first IBIS models for the 82420 and 82430 PCIset components, which operate at speeds up to 66 MHz. Models of additional Intel chip sets and processors will be available soon.

"Accurate signal integrity analysis is virtually impossible without quality models," said John Isaac, director of marketing for Mentor Graphics' PCB Division, San Jose, Calif. "IBIS is the first step toward providing critical behavior information required for complex systems, and it will significantly increase the productivity of high-speed board and MCM designers."

Participating Companies Form IBIS Open Forum

The IBIS Version 1.1 specification was developed through the cooperative efforts of simulator vendors and semiconductor companies who together comprise the IBIS Open Forum. The following participating companies and organizations support the specification: ANACAD Electrical Engineering Software; AnSoft Corporation; Atmel Corporation; Cadence Design Systems; CONTEC Microelectronics U.S.A. Inc.; High Design Technology; HyperLynx; Integrity Engineering, Inc.; Intel Corporation; Interconnectix, Inc.; Intergraph Electronics; intuSoft; Logic Modeling Corporation; Mentor Graphics Corporation; Meta-Software; MicroSim Corporation; North Carolina State University; Performance Signal Integrity; Quad Design Technology; Quantic Laboratories Inc.; Siemens Nixdorf Infromationssyteme AG/Cadlab; and Zeelan Technology, Inc.

"The widespread support for this new specification removes the barriers that have prevented semiconductor vendors from supplying accurate signal integrity models to their customers," said Will Hobbs, models manager for Intel's Xcceleration Tools Group. "Accuracy, speed of development, speed of execution, protection of intellectual property and support by virtually the entire simulator industry are keys to this breakthrough."

Group Plans to Formalize Standard in 1994

Although initially focused on CMOS technologies, the IBIS Open Forum is taking steps to broaden the specification into other technologies and circuits, such as ECL devices and open collector outputs. Such extensions are not perceived to be difficult and are expected to be added quickly. The group intends to develop a robust, comprehensive standard by mid-1994 that can be taken to the standards community for formal adoption. The forum is actively seeking additional participation to support the expansion, especially from semiconductor developers and system designers.

"The combination of IBIS models and compatible software tools will give every engineer the ability to simulate their signal-integrity problems," said Kellee Crisafulli, president of HyperLynx, Inc.

For More Information

For more information about the IBIS Open Forum, send an e-mail request to ibis-info@vhdl.org or call Karen Kirkpatrick, Cadence Design Systems, (508) 262-6448. All of the documents and publicly available models are currently accessible via the public repository of VHDL International's Internet based machine (vhdl.org, 198.31.14.3). FTP, Gopher and public dial-in access methods are all supported.

###

IBIS Open Forum
Contact List

Company:	**Contact Name:**	**Phone Number:**	**Fax Number:**
ANACAD Electrical Engineering Software	Peter Denyer	(408) 954-0600	(408) 954-8884
Ansoft Corporation	Keith Franz	(412) 261-3200	(412) 471-9427
Atmel Corporation	Dan Terry	(408) 436-4346	(408) 436-4200
Cadence Design Systems	Laurel Stanley	(508) 262-6104	(508) 262-6777
CONTEC Microelectronics U.S.A. Inc.	Dr. Paul Wang	(408) 434-6767	(408) 434-6884
High Design Technology	Michael Smith	(408) 954-0600	(408) 954-8884
HyperLynx	Kellee Crisafulli	(206) 869-2320	(206) 881-1008
Integrity Engineering, Inc.	Greg Doyle	(612) 636-6913	(612) 631-2241
Intel Corporation	Will Hobbs	(503) 696-4369	(503) 696-4210
Interconnectix, Inc.	Bob Ross	(503) 684-6641	(503) 639-3469
Intergraph Electronics	John Prince	(205) 730-8135	(205) 730-8344
intusoft	Charles Hymowitz	(310) 833-0170	(310) 833-9658
Logic Modeling Corporation	Randolph Harr	(408) 957-5241	(408) 945-9181
Mentor Graphics Corporation	Ravender Goyal	(503) 685-7000(2242)	(503) 685-7839
Meta-Software	Cindi Maciolck	(408) 369-5440	(408) 371-5638
MicroSim Corporation	Denise Dres	(800) 245-3022	(714) 455-0554
North Carolina State University	Michael Steer	(919) 515-5191	(919) 515-5523
Performance Signal Integrity	Casey Jones	(412) 682-7101	(412) 682-7178
Quad Design Technology	Jon Powell	(805) 988-8250	(805) 988-8259
Quantic Laboratories Inc.	Mike Ventham	(204) 942-4000	(204) 957-1158
Siemens Nixdorf Infromationssysteme AG/Cadlab	Werner Rissiek	49-5251-284-155	49-5251-284-105
Zeelan Technology, Inc.	Hiro Moriyasu	(503) 520-1000	(503) 520-1001