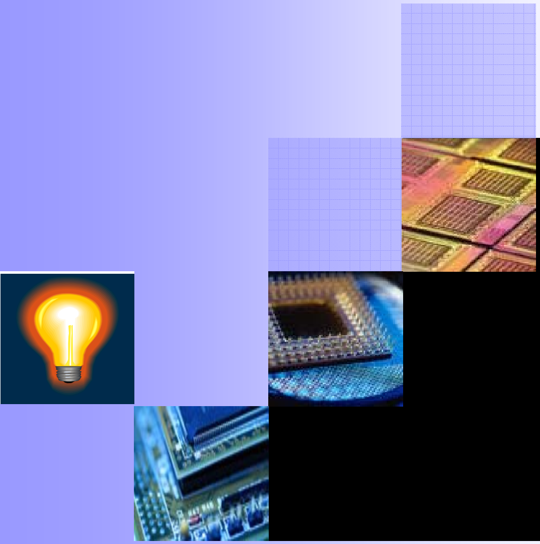


Proper IBIS Package Modeling Techniques and Usage in Ideal PDS and SSO Simulations

Sam Chitwood
FAE Manager

IBIS Summit
February 7, 2008

Outline

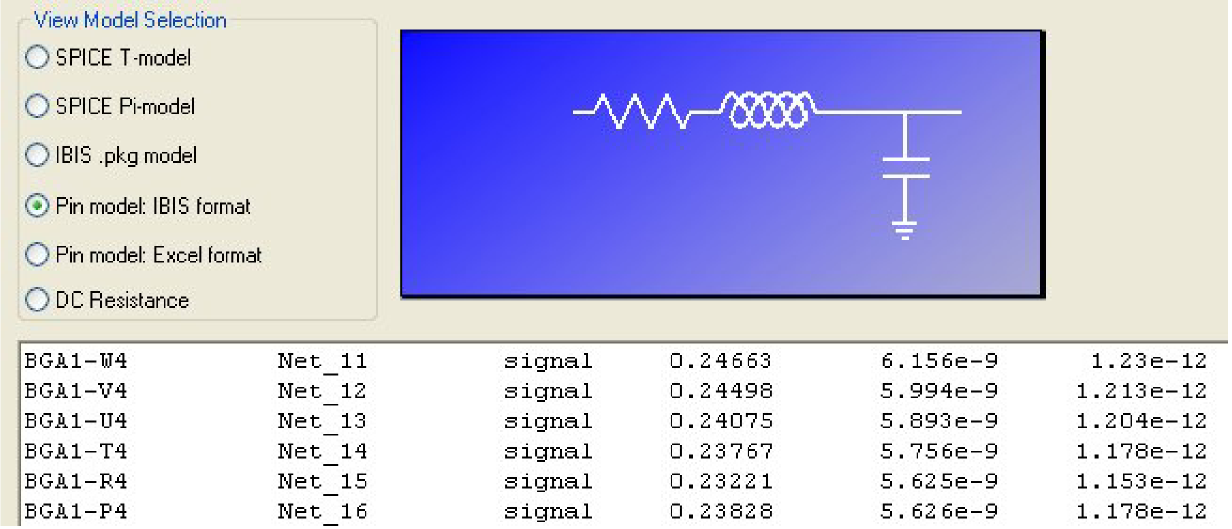
- Assumptions in IBIS Package Models
- The [Pin] Model
  - Inherent limitations and their implications
  - Extraction techniques for Ideal-PDS applications
- The [Define Package Model]
  - What a difference coupling can make…
  - Extraction techniques for SSO applications
- PDS Connectivity at the Die (and Board)
- IBIS Pkg Model Accuracy – How high can we go?
- Summary
- Acknowledgements and References

Assumptions in IBIS Package Models

- 1:1 relationship between die pads and board pins
  - No signal net branching is allowed
  - Multiple die not supported
  - Also applies to POWER and GND nets
- RLCs are allowed for POWER and GND pins
- [Pin Mapping] connects PU, PD, and clamps to actual POWER and GND locations
  - Should be used in realistic PDS situations
  - Generally agreed that these links are at the die side
  - This connection is “ideal” (no die parasitics assumed)
  - Multiple physical die pads can become one logical circuit terminal in simulation
- *This document’s modeling techniques assume package POWER and GND nets have multiple die pads, board pins, and “plane” routing.*

The [Pin] List and Package Model

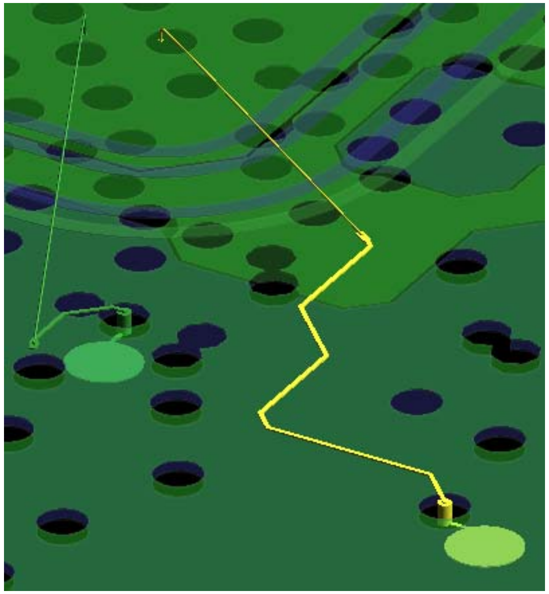
- Associates I/O models to pins and signal names.
- Should list ***ALL*** board pins! Unfortunately POWER and GND pins are sometimes omitted.
- R_pin, L_pin, and C_pin are allowed for all pins.
- No mechanism to include coupling (mutual terms).



View Model Selection

○ SPICE T-model
○ SPICE Pi-model
○ IBIS .pkg model
● Pin model: IBIS format
○ Pin model: Excel format
○ DC Resistance

```
BGA1-W4      Net_11      signal    0.24663     6.156e-9    1.23e-12
BGA1-V4      Net_12      signal    0.24498     5.994e-9    1.213e-12
BGA1-U4      Net_13      signal    0.24075     5.893e-9    1.204e-12
BGA1-T4      Net_14      signal    0.23767     5.756e-9    1.178e-12
BGA1-R4      Net_15      signal    0.23221     5.625e-9    1.153e-12
BGA1-P4      Net_16      signal    0.23828     5.626e-9    1.178e-12
```



Limitations of [Pin] for PDS Modeling

- PDS nets do not have a 1:1 pad-pin ratio.
- Because the [Pin] model does not allow coupling between PDS pins, an accurate per-pin PDS [Pin] model is virtually impossible to construct (see references).
- If RLCs for POWER and GND pins are present, how should they be interpreted? These partials have no mutuals to relate them, thus no loops can be inferred.
- What does your ideal-PDS PCB SI tool do with the GND and “global ground” nodes shown in the figure?
- What does the GND pin capacitance represent? You cannot measure this.
- Therefore, the [Pin] package model should be extracted for one application only:

Ideal PDS simulations

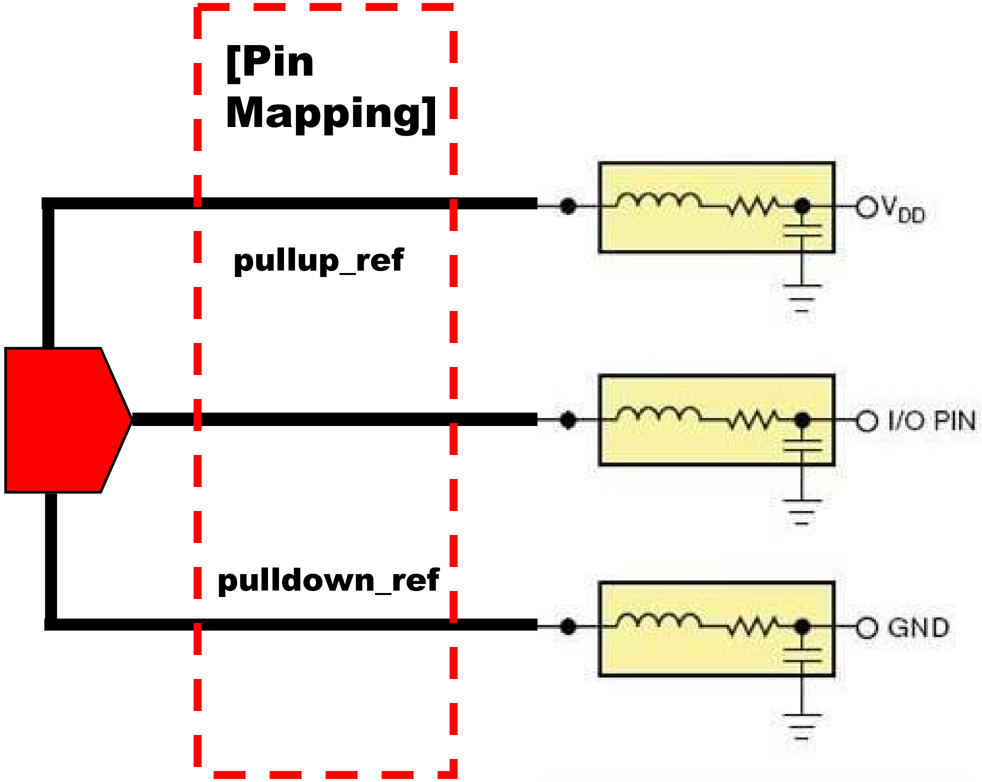
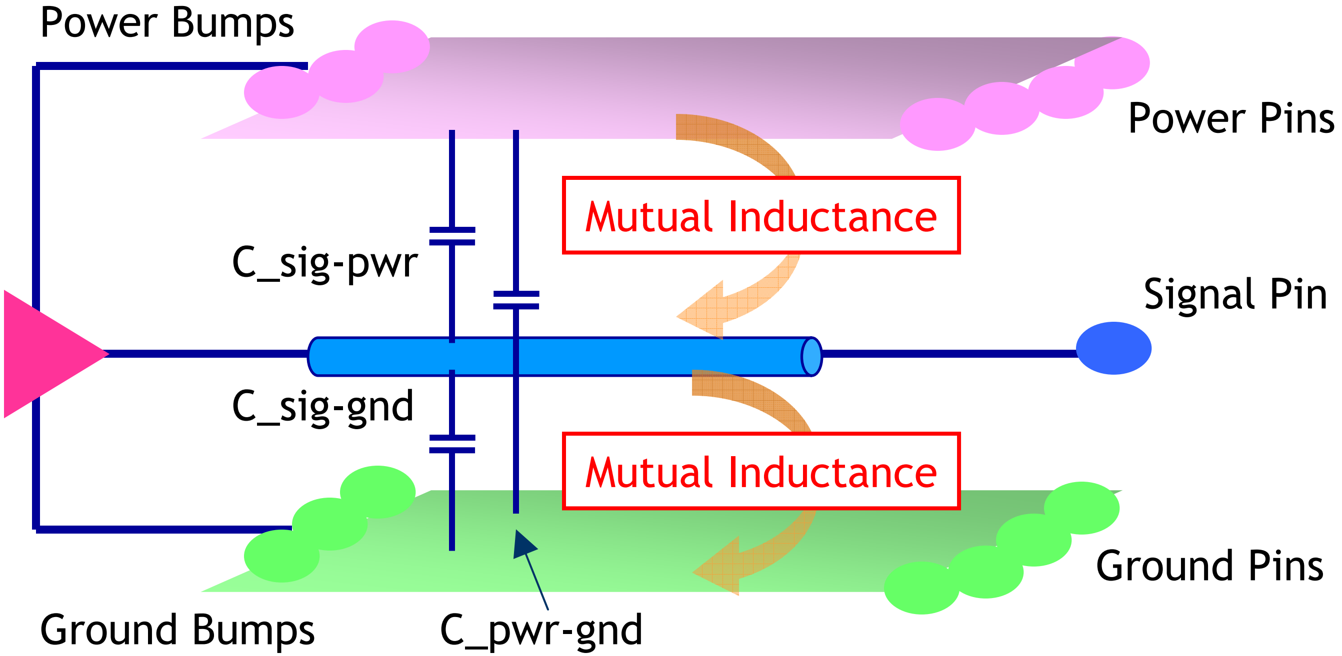


Fig 1. An incorrect [Pin] model containing per-pin POWER and GND RLC entries.

Unfortunately the [Pin] example in the IBIS spec encourages this practice and many IBIS users expect to see these entries.

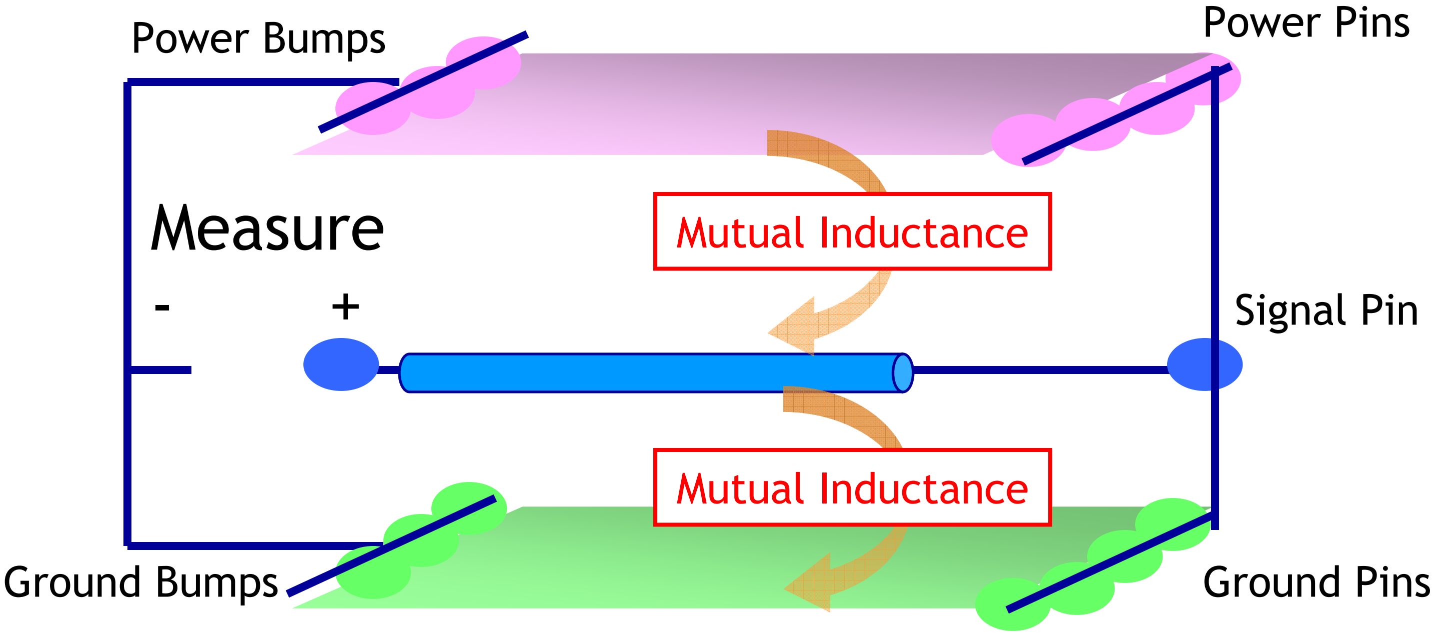
Limitations of [Pin] for Signal Modeling

Package Geometry (Simplified)



- Signal C_pin has the ***exact same problem*** that C_comp has in realistic PDS simulations! For an accurate description, we must know the split between C_sig-pwr and C_sig-gnd.
- Since no mutual inductance can exist between signal and POWER or GND pins, signal return paths cannot be inferred from the model. Return current could be on POWER, GND, or both.
- Is R_pin at DC or x MHz to consider skin effect? How to handle the return path’s impact?

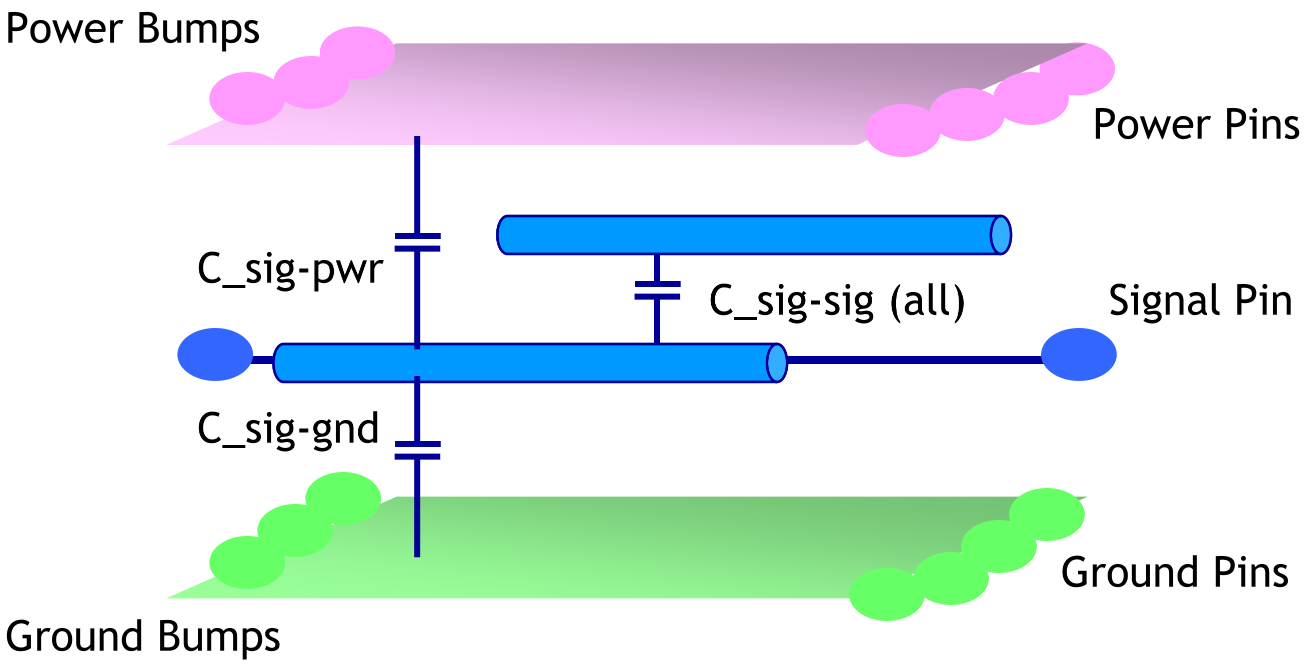
[Pin] Inductance and Resistance Extraction



- Making the assumption that the [Pin] model will be used in ideal-PDS simulations solves many of the problems with this model. *No RLCs should be present in POWER or GND pins.*
- Signal pin inductance is now L_loop. It assumes all POWER and GND nets are AC-shorted at the pad and pin sides (as they will be in their intended ideal-PDS SI simulations).
- Signal pin resistance is also R_loop. There is no “correct” frequency for extraction.

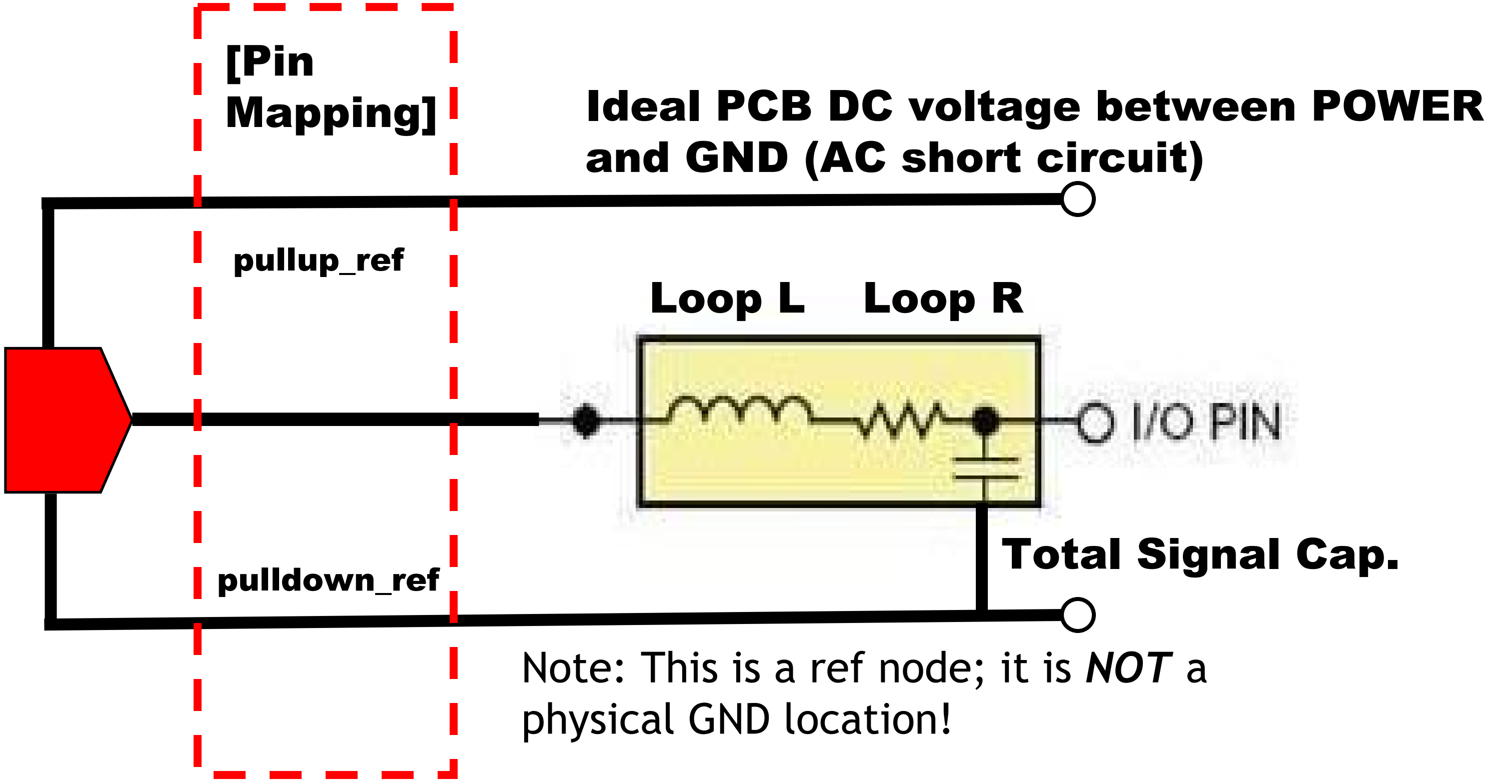
[Pin] Model Capacitance Extraction

Package Geometry (Simplified)



- Signal pin capacitance is now C_total = C_sig-pwr + C_sig-gnd + C_sig-sig (all).
- This model assumes all POWER and GND nets are AC-shorted at the pad and pin sides (as they will be in their intended ideal-PDS SI simulations).
- C_sig-sig (all) is usually much smaller than C_sig-pwr + C_sig-gnd, but should be included under the assumption that neighboring nets are held quiet high or low.

Correct Usage of the [Pin] Model



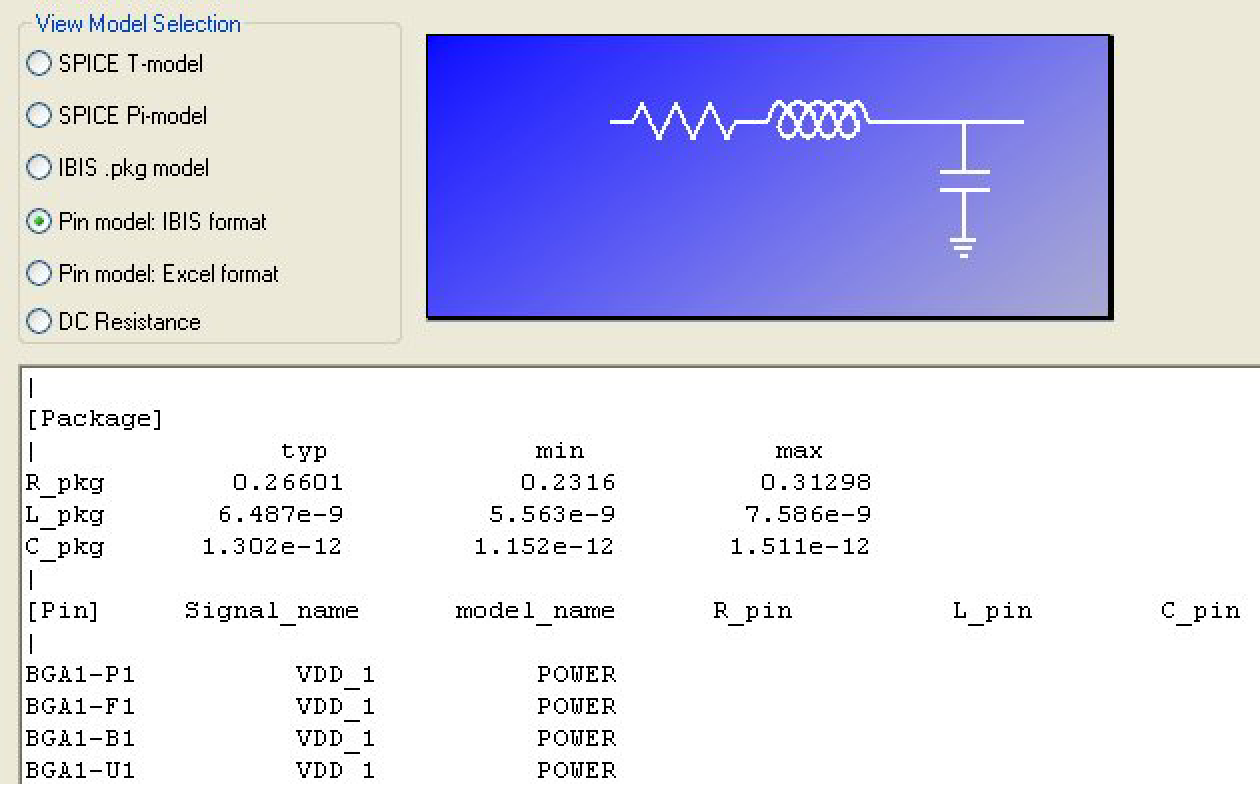
Ideal PCB DC voltage between POWER and GND (AC short circuit)

Note: This is a ref node; it is *NOT* a physical GND location!

- This [Pin] model implementation allows simple connection of driver, receiver, and PCB models.
- The pulldown node becomes a "ref" node and makes voltage measurement easy.
- These package values are physical quantities that can be measured and correlated.
- [Pin Mapping] is shown for completeness, but its use is irrelevant in this situation.

A note about [Package]

- Intended to quickly identify the numerical min. and max. RLC values of the [Pin] list
- If POWER & GND RLCs are in the [Pin] list, [Package] should consider these values
- Not recommended for any simulation unless no other model is available



View Model Selection

○ SPICE T-model
○ SPICE Pi-model
○ IBIS .pkg model
● Pin model: IBIS format
○ Pin model: Excel format
○ DC Resistance

```
|
[Package]
|                typ              min              max
R_pkg         0.26601           0.2316          0.31298
L_pkg        6.487e-9        5.563e-9          7.586e-9
C_pkg       1.302e-12       1.152e-12         1.511e-12
|
[Pin]       Signal_name       model_name       R_pin         L_pin         C_pin
|
BGA1-P1              VDD_1           POWER
BGA1-F1              VDD_1           POWER
BGA1-B1              VDD_1           POWER
BGA1-U1              VDD 1           POWER
```

The [Define Package Model]

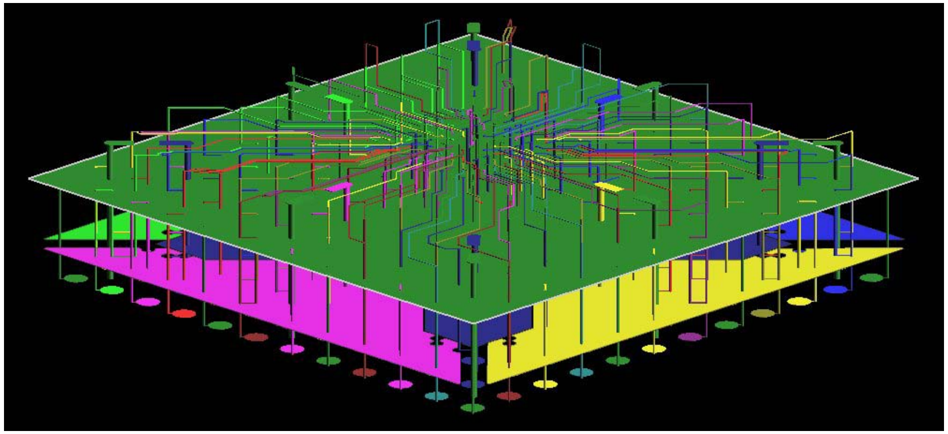
- Typically delivered in a separate .pkg file
  - Facilitates separate I/O and pkg modeling efforts
- Two types: [Number of Sections] and [Model Data]
- [Number of Sections] technique essentially makes the same assumptions as [Pin] models
  - No coupling allowed > for ideal-PDS simulations only
  - L and R are loop values, C is total
  - Fork option allows modeling of package stubs
- [Model Data] utilizes R, L, and C matrices
  - Coupling (mutuals) can finally be defined between pins!
  - Sparse matrices can be used to simplify model complexity
  - Ensure model passivity if coupling terms are removed

[Model Data] Extraction Methodology

- Although matrix coupling facilitates per-pin PDS modeling, it is not generally recommended because:
  - The 1:1 pad-pin ratio is still (incorrectly) assumed
  - The number of coupling terms would be excessively large
  - Mutual resistance terms are not supported in some tools
- The PDS model extraction should lump all POWER net pins on a per-net basis
  - For example, if VDD5 has 5 pins it should only have 1 logical pin in the [Model Data] pin list
- Pick one GND reference net that will NOT appear in the list of [Model Data] pins
  - This net will become the “ref” node of the final circuit
  - All L and R values in the matrix are loop WRT this net
  - Diagonal capacitance matrix terms are $C\_{\text{net-GND}}$.

[Model Data] Extraction Methodology

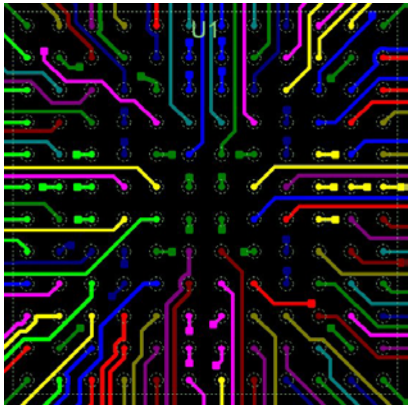
Assume **16 signal nets** of the package are of interest for simplicity of discussion. The PDS nets will also be modeled, including all necessary coupling terms.



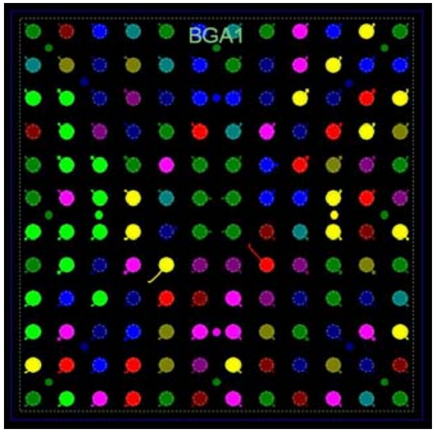
Top of Package:

- All **POWER pins are lumped** as a positive node.
- All **GND pins are lumped** as a negative (or reference) node.
- **Port 1** is defined between the positive node and the reference node.
- **Ports 2 ~ 17** are defined between corresponding signal pins and the reference node, which is the ground of the package.

Package Top



Package Bottom

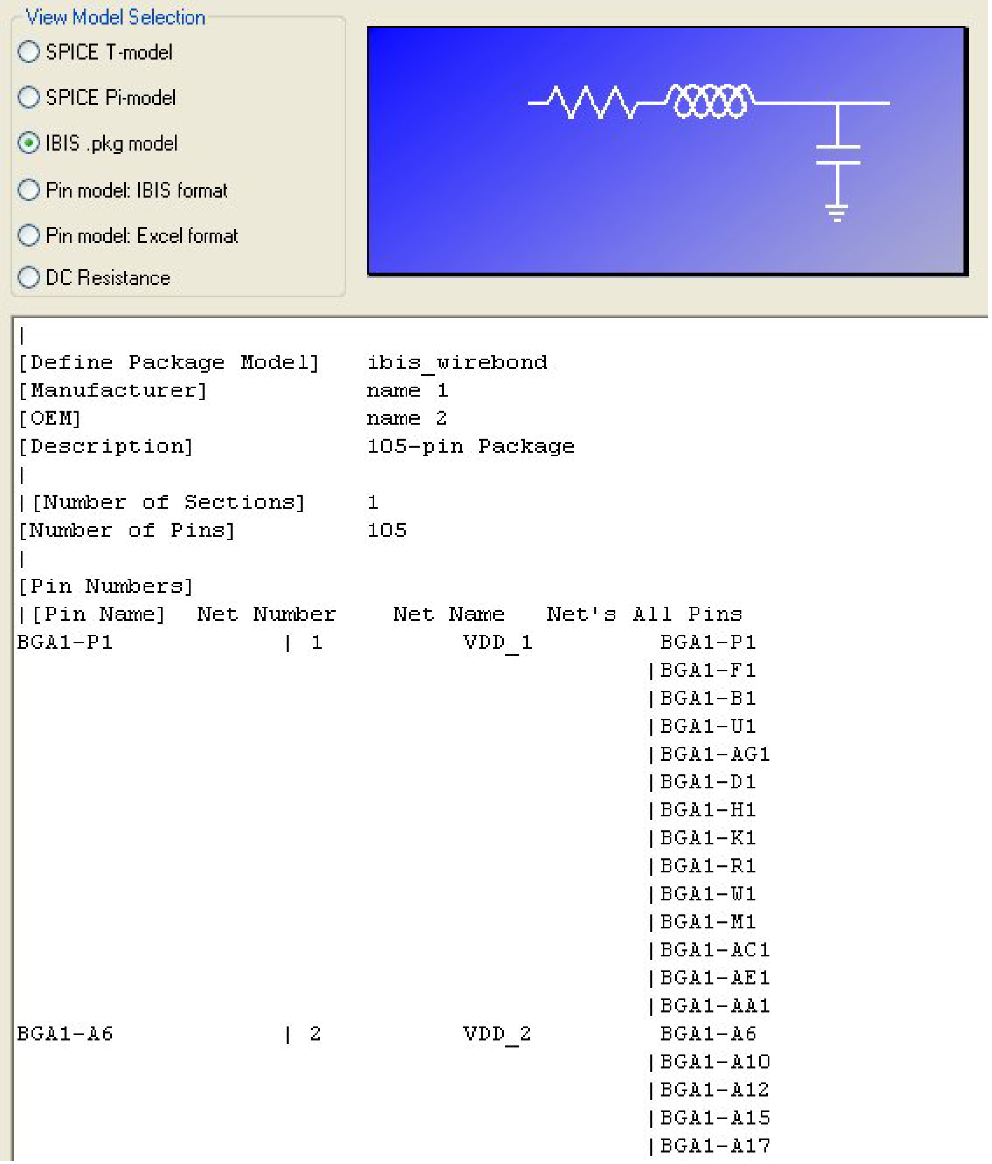


Bottom of Package:

- All **POWER pins are lumped** as a positive node.
- All **GND pins are lumped** as a reference node.
- **Port 18** is defined between the positive node and the reference node.
- **Ports 19 ~ 34** are defined between corresponding signal pins and the reference node, which is the ground of the package.

Example Pin List Using Lumped Pins

- Net VDD_1 has multiple pins, but only pin BGA1_P1 is listed. The same concept applies for net VDD_2.
- The package has more than 105 physical pins, but this is the number of logical circuit terminals.
- The GND net will not have an explicit pin in the list.

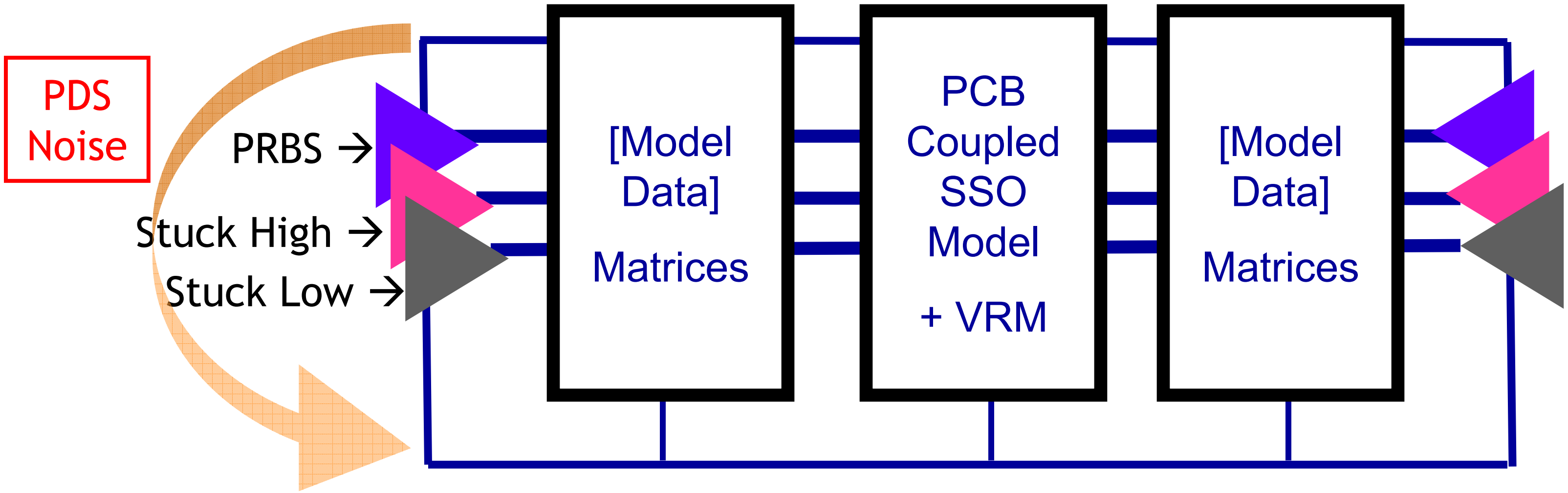


View Model Selection

○ SPICE T-model
○ SPICE Pi-model
● IBIS .pkg model
○ Pin model: IBIS format
○ Pin model: Excel format
○ DC Resistance

```
|
[Define Package Model]    ibis_wirebond
[Manufacturer]            name 1
[OEM]                     name 2
[Description]             105-pin Package
|
|[Number of Sections]     1
[Number of Pins]          105
|
[Pin Numbers]
|[Pin Name]   Net Number    Net Name   Net's All Pins
BGA1-P1              | 1          VDD_1          BGA1-P1
                                                |BGA1-F1
                                                |BGA1-B1
                                                |BGA1-U1
                                                |BGA1-AG1
                                                |BGA1-D1
                                                |BGA1-H1
                                                |BGA1-K1
                                                |BGA1-R1
                                                |BGA1-W1
                                                |BGA1-M1
                                                |BGA1-AC1
                                                |BGA1-AE1
                                                |BGA1-AA1
BGA1-A6              | 2          VDD_2          BGA1-A6
                                                |BGA1-A10
                                                |BGA1-A12
                                                |BGA1-A15
                                                |BGA1-A17
```

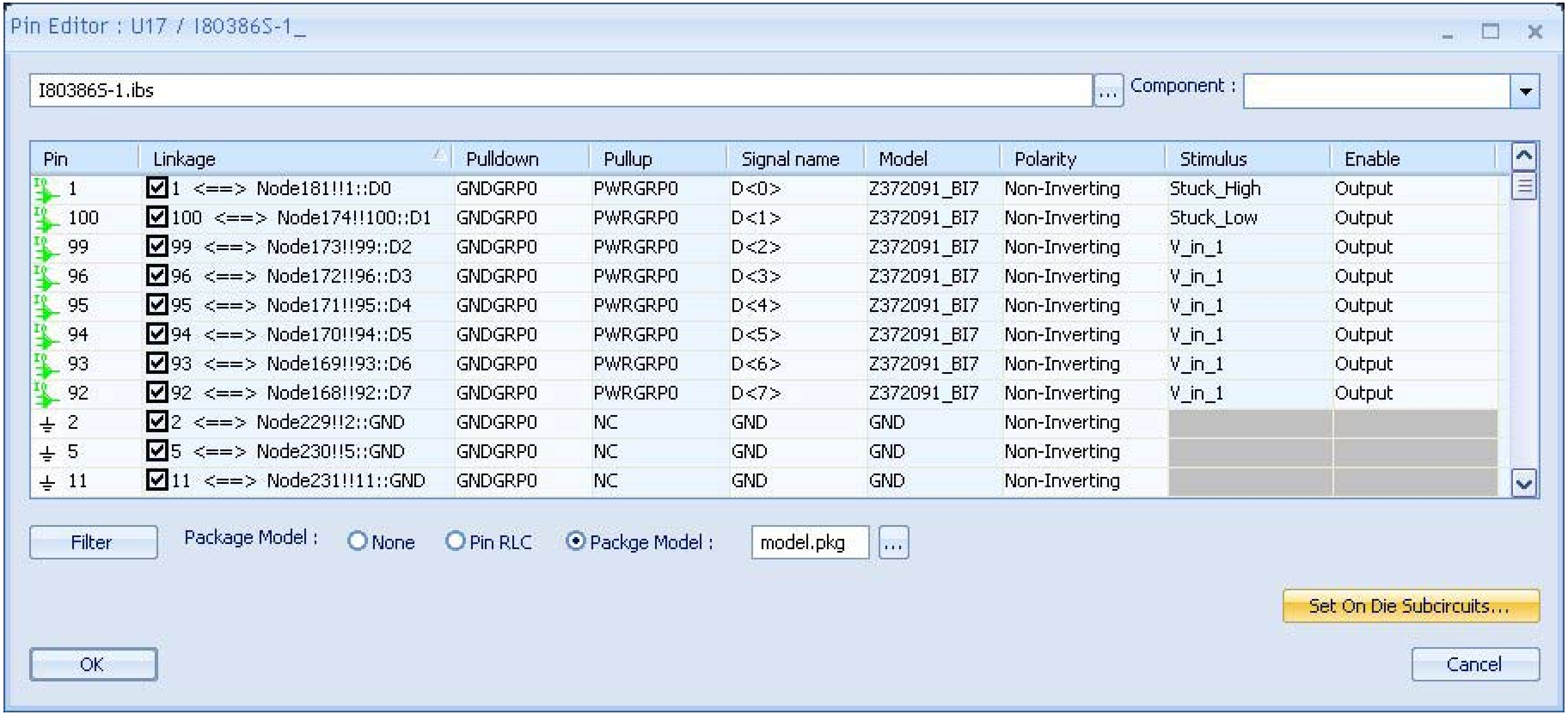
Correct Usage of [Model Data]



Note: This is a ref node; it is ***NOT*** a physical GND location!

- This [Model Data] example shows the connections of driver, receiver, and PCB models.
- The pulldown node becomes the “ref” node and makes voltage measurement easy.
- The package values are physical quantities that can be measured and correlated.
- [Pin Mapping] must be used to make the PU, PD, and clamp connections to the logical POWER terminal and the “ref” node (GND net). The EDA tool must support this technique.

Connectivity at the Die: [Pin Mapping]



Pin Editor : U17 / I80386S-1_

I80386S-1.ibs ... Component :

Pin	Linkage	Pulldown	Pullup	Signal name	Model	Polarity	Stimulus	Enable
1	☑ 1 <==> Node181!!1::D0	GNDGRP0	PWRGRP0	D<0>	Z372091_BI7	Non-Inverting	Stuck_High	Output
100	☑ 100 <==> Node174!!100::D1	GNDGRP0	PWRGRP0	D<1>	Z372091_BI7	Non-Inverting	Stuck_Low	Output
99	☑ 99 <==> Node173!!99::D2	GNDGRP0	PWRGRP0	D<2>	Z372091_BI7	Non-Inverting	V_in_1	Output
96	☑ 96 <==> Node172!!96::D3	GNDGRP0	PWRGRP0	D<3>	Z372091_BI7	Non-Inverting	V_in_1	Output
95	☑ 95 <==> Node171!!95::D4	GNDGRP0	PWRGRP0	D<4>	Z372091_BI7	Non-Inverting	V_in_1	Output
94	☑ 94 <==> Node170!!94::D5	GNDGRP0	PWRGRP0	D<5>	Z372091_BI7	Non-Inverting	V_in_1	Output
93	☑ 93 <==> Node169!!93::D6	GNDGRP0	PWRGRP0	D<6>	Z372091_BI7	Non-Inverting	V_in_1	Output
92	☑ 92 <==> Node168!!92::D7	GNDGRP0	PWRGRP0	D<7>	Z372091_BI7	Non-Inverting	V_in_1	Output
2	☑ 2 <==> Node229!!2::GND	GNDGRP0	NC	GND	GND	Non-Inverting		
5	☑ 5 <==> Node230!!5::GND	GNDGRP0	NC	GND	GND	Non-Inverting		
11	☑ 11 <==> Node231!!11::GND	GNDGRP0	NC	GND	GND	Non-Inverting		

Filter   Package Model : ○ None ○ Pin RLC ● Packge Model : model.pkg ...

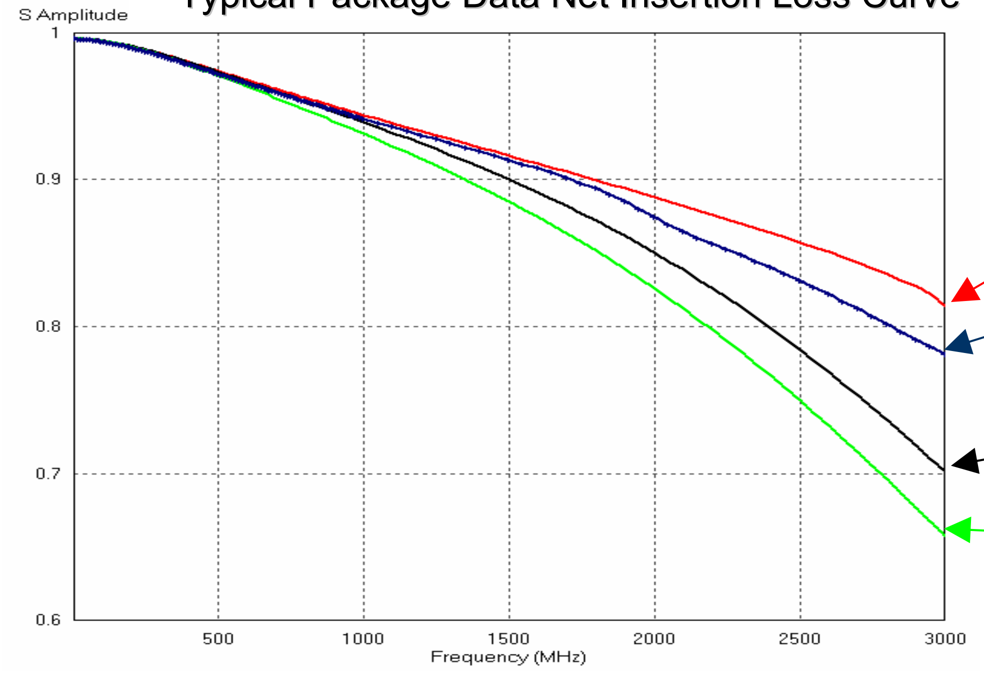
Set On Die Subcircuits...

OK   Cancel

- This window shows the necessary setup items for a complete SSO analysis.
- Note the highlighted button that allows assignment of On Die Subcircuits - the EDA tool must allow access to the pullup and pulldown nodes. (Since there is not direct access to these nodes in the IBIS file, the on-die PDS model cannot be embedded in the IBIS file.)
- Special handling is needed at the pin side to lump the PCB terminals to match the .pkg model.

IBIS Package Model Accuracy

Typical Package Data Net Insertion Loss Curve

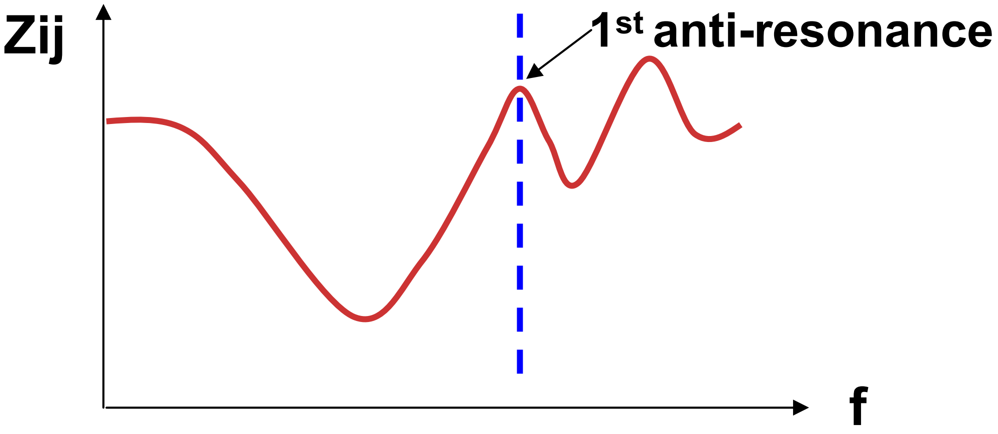


Actual Net Performance

Optimized Broadband 3-section

Optimized Broadband 1-section

Un-optimized RLC circuit (IBIS)



- IBIS PKG models are the least complex but have the least bandwidth
- An IBIS PDS model is generally acceptable to the first unloaded resonance. PKG decaps reduce this.
- Comparison against actual package S-parameters is the best metric.

Summary

- The IBIS package model specifications contain a number of assumptions and nuances that should be thoroughly understood to build accurate models
- This presentation examined issues and modeling techniques for packages with multiple pad/pin PDS nets and “plane” routing
- The [Pin] Model should be used for ideal-PDS simulations only
  - No RLCs should be present in POWER or GND pins
  - Signal pin RLCs should be loop values – not partials
- [Model Data] matrices can include the coupling necessary to build models for SSO analysis
  - POWER and GND terminals should be lumped to reduce model complexity and avoid potential tool issues with mutual resistance
  - The loop modeling concept should also be utilized in this model
- PDS connectivity at the die and board must be carefully managed
- IBIS package model bandwidth is limited by structure resonances
  - Comparison with actual S-parameter response is recommended

Acknowledgement of Sigrity Contributors That Made This Presentation Possible

Mr. Brad Brim
Mr. Jack W. C. Lin
Ms. Yinglei Ren
Ms. Tao Xu
Mr. Gang Kang

References

1. **Fundamentals of S-Parameter Modeling for Power Distribution System (PDS) and SSO Analysis**. IBIS Summit, June 2005.
2. **Issues with Interfacing "2N" and "N+ref" Behavioral Models**. IBIS Summit, June 2005.
3. **System System-Level SSO Simulation Techniques with Various IBIS Package Models**. IBIS Summit, October 2006.
4. Thierauf, Stephen C. ***High-Speed Circuit Board Signal Integrity***. Artech House Publishers, 2004. Pages 20-22.

Thank You!