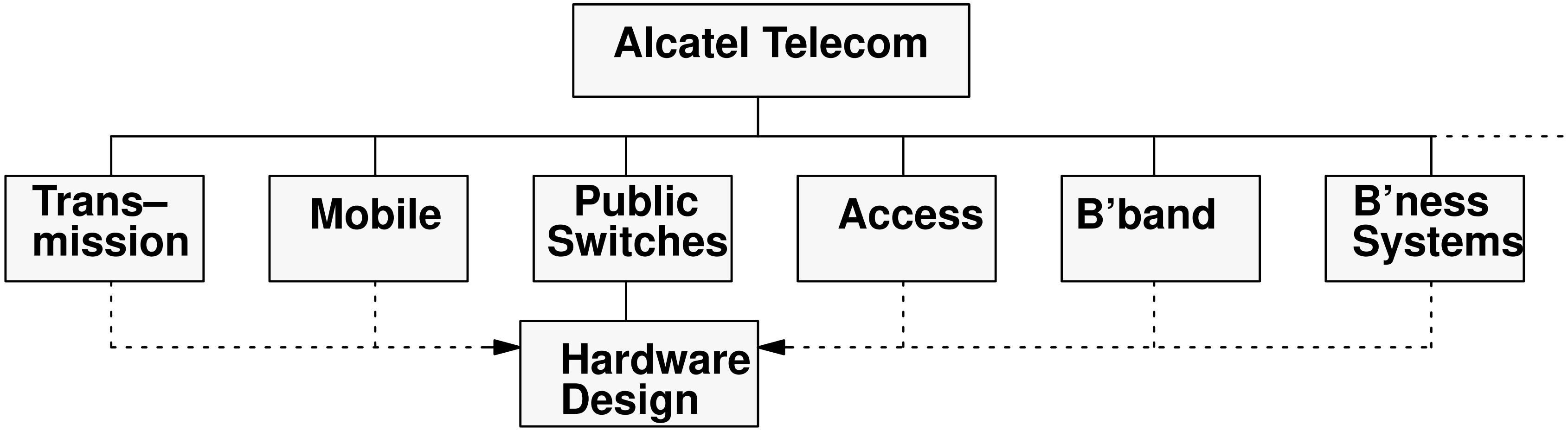
Introduction
Alcatel IBIS Presentation



Board types:

POTS and ISDN subscriber boards

680x0, Intel and PowerPC controller boards

ATM switch

ATM subscriber boards

SDH/PDH repeaters and multiplexers

Passive backplanes

Why Alcatel is represented here today

– The IBIS approach corresponds closely to our traditional way of working:
  - Bergeron diagram analysis
  - Spice simulation using behavioural models
  - Design Rules

– We want to use IBIS for more that just simulating a board.

– A large investment is needed to build and manage a library of IBIS models.
  We must be sure that it's money well spent!

– Model availability is still a major issue.
  We've had problems, so would like to know how the situation can be improved.

– Our design methodology is being modified to include electrical simulation.
  Discussions here should help get ideas on how to optimize this.

– And it's good to be able to put faces to e–mail addresses ......

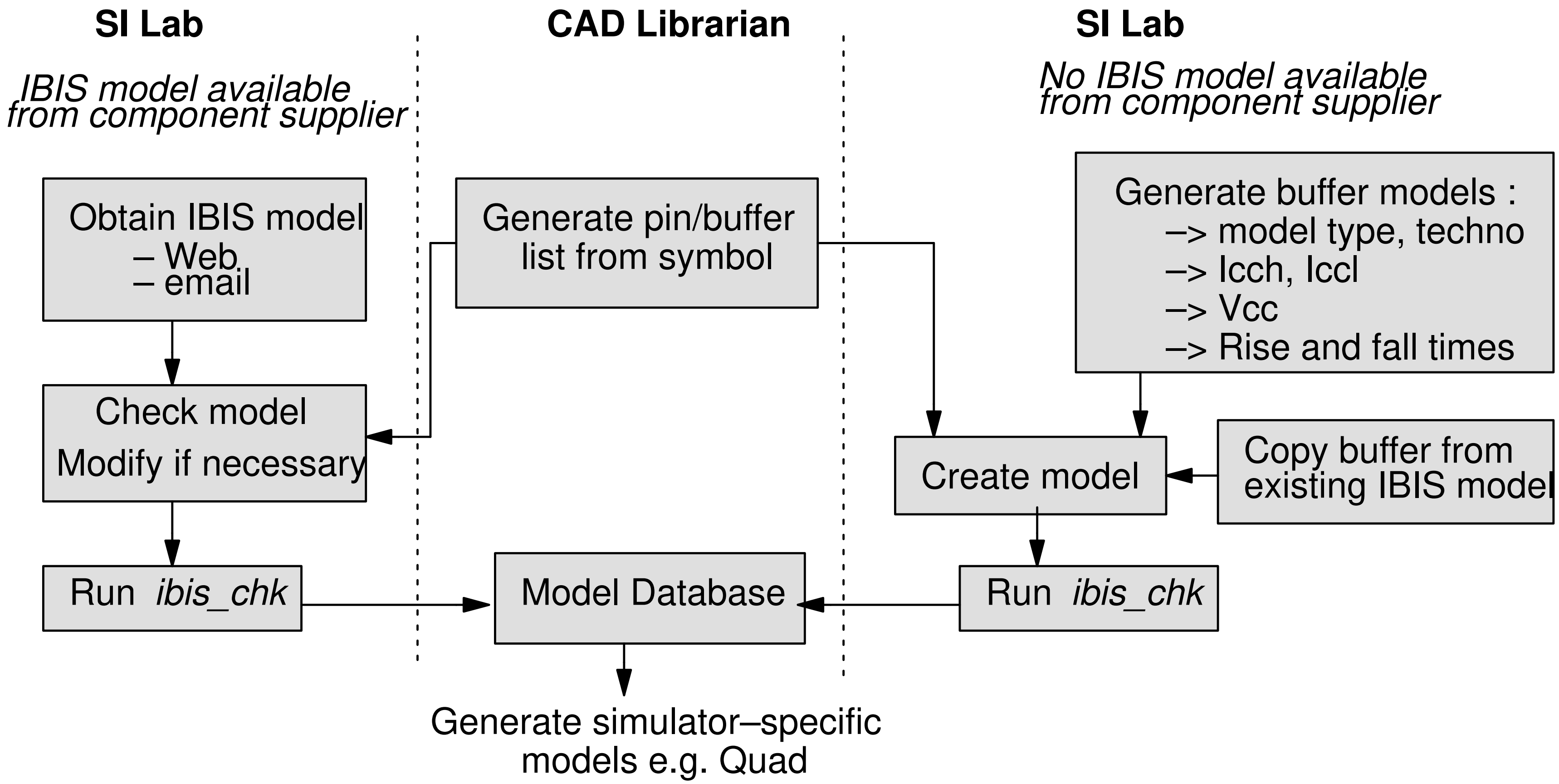
First practical experience

The first board intensively simulated taught us many lessons about IBIS:

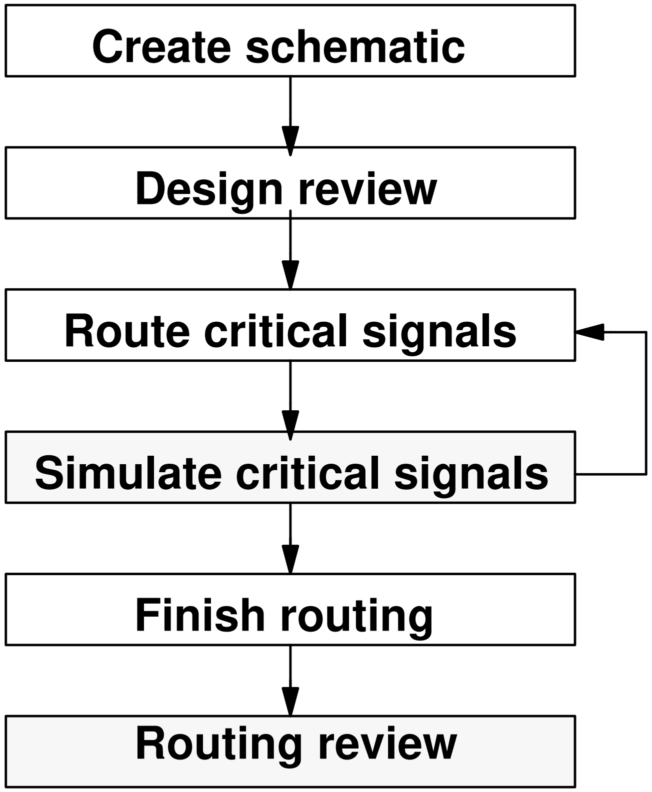
- **IBIS models are still difficult to obtain from component suppliers.**
  However all suppliers are now aware of the IBIS standard.
- **All models contained one or more errors**
  e.g. wrong current polarity, incorrect slewrate, pullup not Vcc referenced, etc.
- **The quality of models varies a lot from vendor to vendor.**
  Some provide full min/max specification, others just typical values.
- **Good models were generated by scaling ”standard” CMOS I/V curves .**
  Need to know Vcc and Icc (short–circuit current), plus rise–time information.

Conclusions: **Need to work closely with suppliers**
All supplier IBIS models need careful review
We will have to generate many models ourselves
Careful control of model revision levels is essential

Introduction of IBIS models into CAD tool chain



1st IBIS application: Post–routing simulation



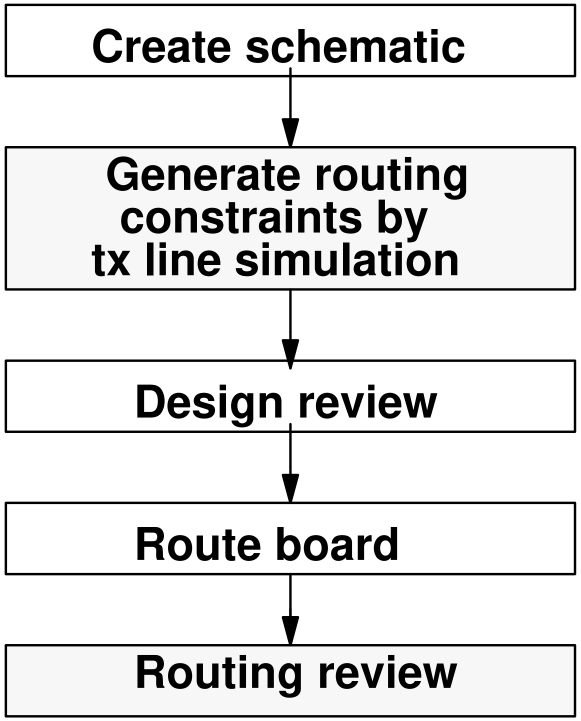
– Identify critical signals
– Apply design rules
(Spice simulation)
– Logic/timing simulation

– Manual routing

– Clean edges
– Time of flight

– Full board simulation

2nd IBIS application: Pre–routing simulation



– Identify critical signals
– Apply design rules
– Logic/timing simulation

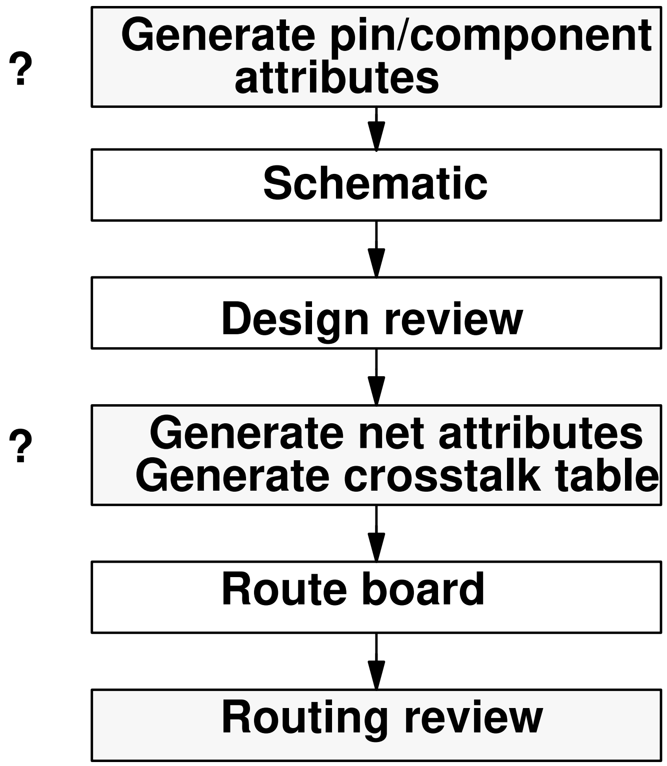
– Estimate routing topology based on component placement

– Constraint driven routing

– Full board simulation

Advantage: design choices made earlier in product cycle

3rd IBIS application: Generation of attributes for design rules



– output impedance
– clamping diodes
– thresholds
– bus–hold, pullups, etc

– Apply design rules
– Logic/timing simulation
– Identify critical signals

– Max voltage swing
– Min transition time
– Min noise margin

– Full board simulation
(transmission + crosstalk)

Advantage: Reduces need for simulation

Important wishes

1) Series components

All IBIS models are in parallel with the signal, pulling it to GND or VCC. This means that certain important components on a high–speed board cannot be modelled:

- **CBT or Quickswitch**
  These are packaged like bus drivers.
- **R, L, C**
  A simulator–independent description would be useful for these components

2) Non–monotonic I/O buffers

It is ***not acceptable*** for a supplier to refuse to provide an IBIS model just because the I/V curves are non–monotonic.

- **Bus–hold**
  Allow small monotonicitiy. The simulator can filter this out if necessary.
- **Controlled slew–rate buffers**
  Define an algorithm or measurement method to generate usable I/V curves

Less important wishes

- **Easier to understand I/V curves**
  Let's get rid of the Vcc dependence of the pullup curves, and the fiddly subtractions needed to get the clamping curves!
  Suggestion: new keywords [Hi–Z], [Lo–Z Pullup], [Lo–Z Pulldown].
- **More background information**
  After the [Note] keyword, could suppliers please include:
  Contact name and address
  Brief description of component, or URL to component description.
- **Unique buffer names**
  Guidelines on buffer naming: each supplier should use a unique, meaningful name.
- **Better model verification**
  There are still too many errors in IBIS models supplied today.

Other wishes

- **Full electrical specification**
  An IBIS file should contain all the information found today in the ”Electrical Specification” chapter of a component datasheet.
- **Paper datasheet**
  It is much easier to review a nicely formatted page generated from an IBIS model than the ASCII file itself.
- **More models!**
  Many suppliers seem hesitant to release models. Let’s make it easier for them to release alpha/beta versions. For example, an alpha model might have typical values only, the beta might have min/max values which are more extreme than the final model.
- **Up–to–date Cookbook**
  This should have a section explaining how to ***rapidy*** generate ***useful*** models.

IBIS as a specification tool

An IBIS file can be used to specify the electrical characteristics of a component:

- **ASICs**
  Generate IBIS model for ASIC before choice of foundry. This model would later guide the choice of buffers from foundry library.
- **Second sourcing**
  When introducing a 2nd source for a component, its IBIS model can be compared with that of the existing component.
- **Industry–standard I/O**
  It would be useful to have ”golden” IBIS models for:
  – standard I/O such as PCI, LVDS, BTL etc
  – commodity technologies e.g. LVT, LVC, AC, Fast, memory

=> Tool needed to compare specification model with actual component model