MIXED-DOMAIN IBIS MODEL EXTRACTION AND IMPLEMENTATION

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PRESENTATION OUTLINES

1-TWO PORT IBIS MODEL FORMULATION

2-OUTPUT PORT FREQUENCY DOMAIN EXTRACTION

3-INPUT PORT TIME DOMAIN EXTRACTION

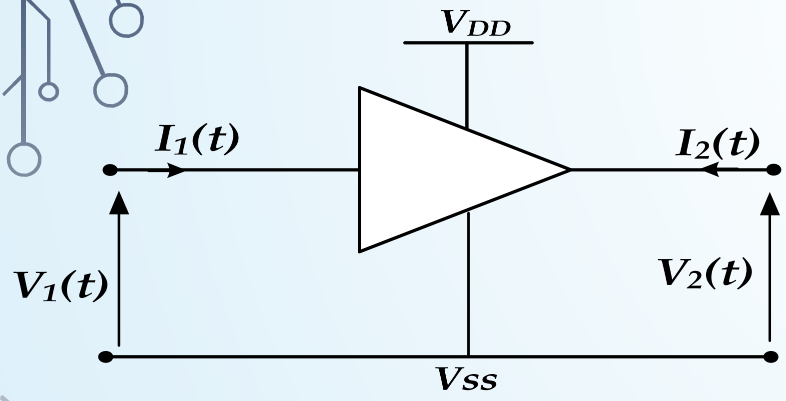
4- PRE-DRIVER MODEL GENERATION AND IMPLEMENTATION

5-GLOBAL MODEL VALIDATION

6-CONCLUSION

EVENT-DRIVEN IBIS MODEL

- Two-port Driver/Receiver :



- The general event-driven and time domain form:

$$I_2(t,n) = F\left(V_1(n), V_2\,(t), \frac{dV_2(t)}{dt}, \dots, \frac{dI_2(t)}{dt}, \dots\right)$$

- IBIS model structure :

$$I_2(t) = w_L^n(t).\, i_L(V_2(t), d/dt) + w_H^n(t).\; i_H(V_2(t), d/dt)$$

- ✓ The output port drives high currents $I_2(t)$ when compared to the negligible $I_1(t)$due to the large size of the last stage transistors: $I_2(t) \gg I_1(t)$.
- ✓ $F(.)$ is a suitable multidimensional nonlinear function.
- ✓ The event *n*, controlled by the IC core variables, $V_1(n)$ and $\mathrm{I}_1(n)$, defines the rising (r) and falling (f) transitions that mark the change between the "high" – *H* and "low" – *L* logic states.

OUTPUT PORT FREQUENCY DOMAIN EXTRACTION

Large-signal I-Q Model

$$I_K(v_2(t)) = I_K^c(v_2(t)) + \frac{dQ_K(v_2(t))}{dt}$$

Small-signal Model (Differentiation)

$$i_k = \frac{\partial I_k^c(V_2)}{\partial V_2} v_2 + j\omega \frac{\partial Q_k(V_2)}{\partial V_2} v_2 \; ; \quad k = L, H$$

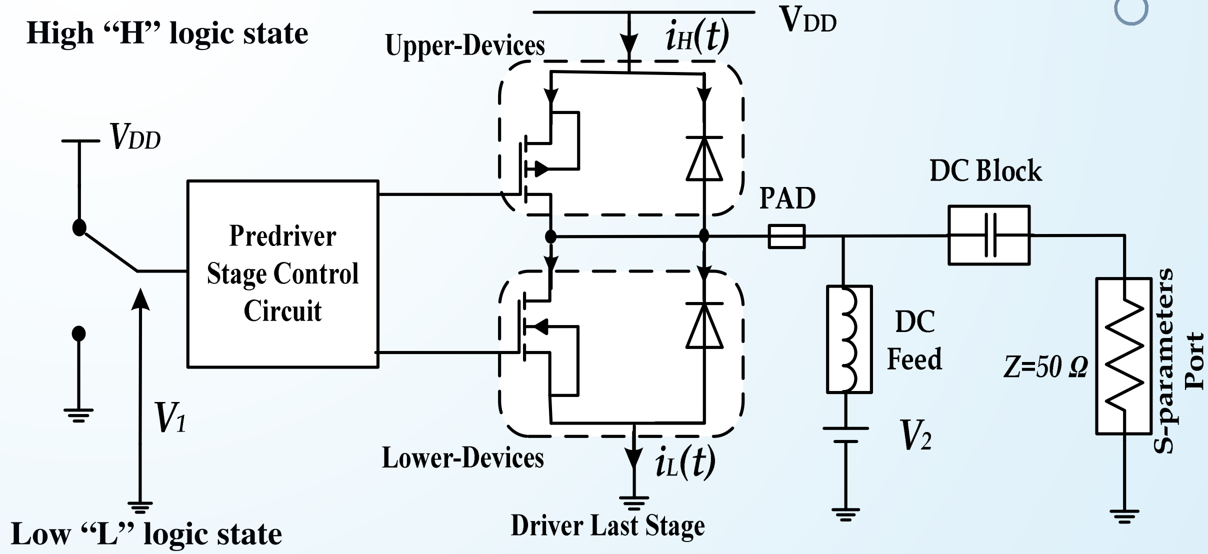
Bias-dependent admittance Y-parameters

$$Y_{22,k}(V_2,\omega) = \frac{i_k}{v_2} = G_k^c(V_2) + j\omega C_k(V_2)$$

Linear regression over frequency range

$$\begin{cases} \frac{\partial Q_k}{\partial V_2} = C_i(V_2) = \frac{1}{2\pi f} Im\left(Y_{22}(V_{1k}, V_2)\right) \\ \frac{\partial I_k^c}{\partial V_2} = g_i^c(V_2) = Re\left(Y_{22}(V_{1k}, V_2)\right) \end{cases}$$

Setup for the bias-dependent Y- parameters Extraction

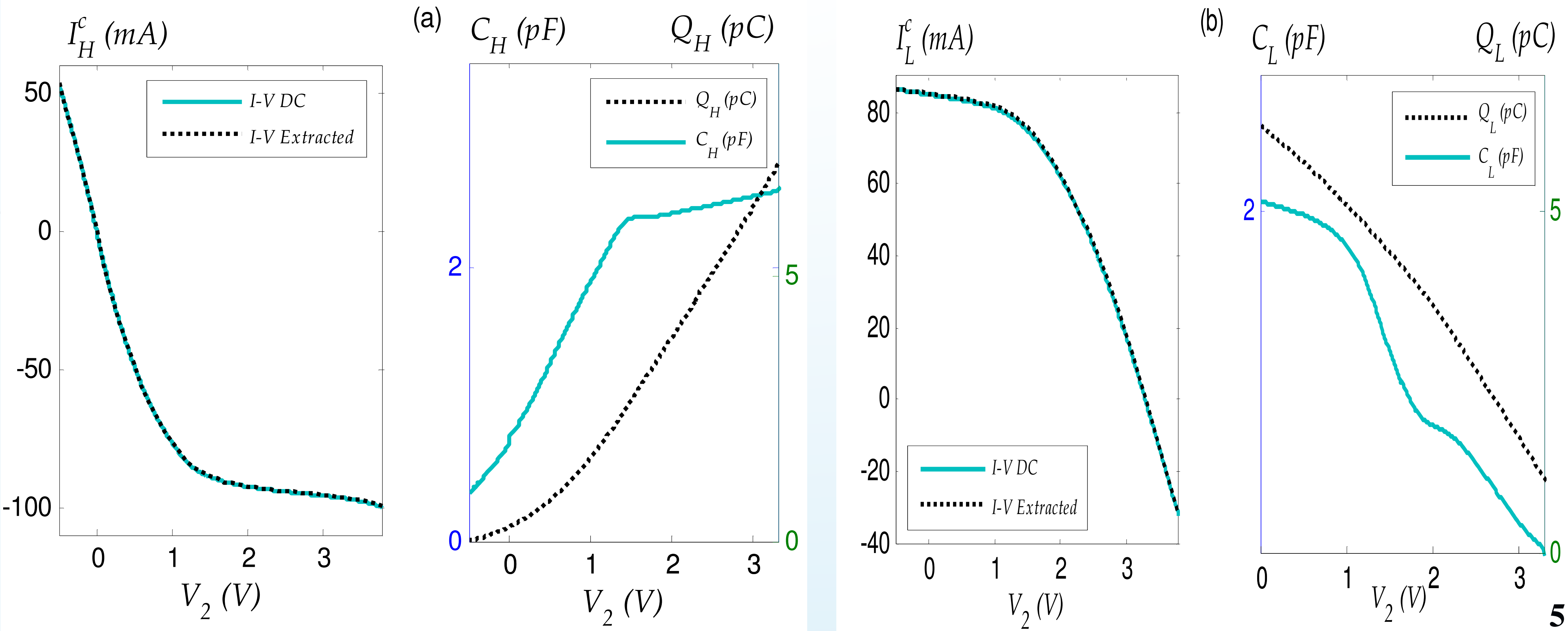


Large-Signal Model (Integration)

$$\begin{cases} I_K^c(V_2) = \int_{-\Delta}^{V_{DD}+\Delta} G_k^c(V_2) dV_2 \\ Q_K(V_2) = \int_{-\Delta}^{V_{DD}+\Delta} C_k(V_2) dV_2 \end{cases}$$

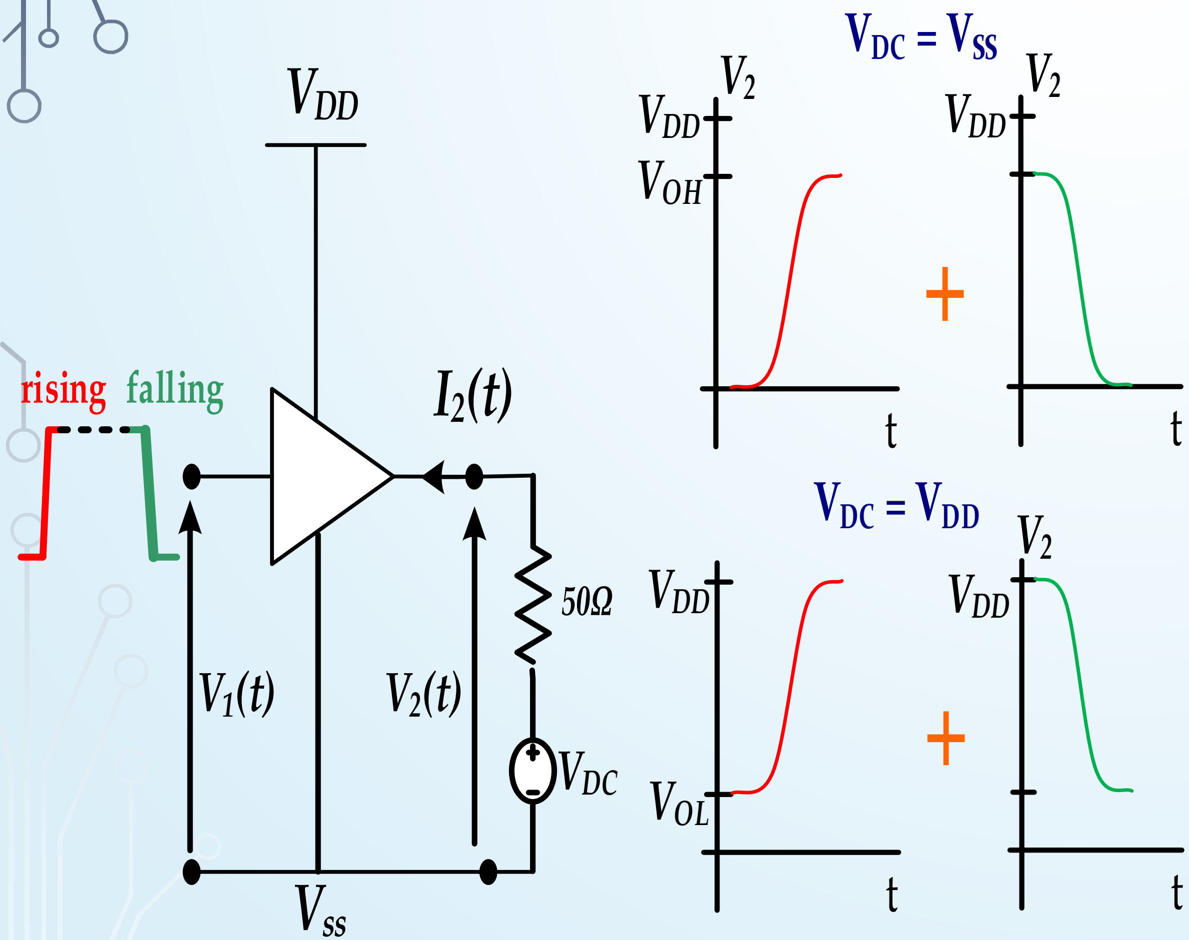
I-Q Model Function's Validations

Comparison of the extracted I-V function with dc measurements and the Q-V function lower (a) and upper (b) devices' functions.



PREDRIVER TIME DOMAIN CHARACTERIZATION

✓ Setup for Timing function extraction



✓ The sequence $\{I_{2,a}(t), V_{2,a}(t)\}$ and $\{I_{2,b}(t), V_{2,b}(t)\}$ are measured for each input edge transitions and for load a, (50Ω)and load b, (50Ω +Vdd)

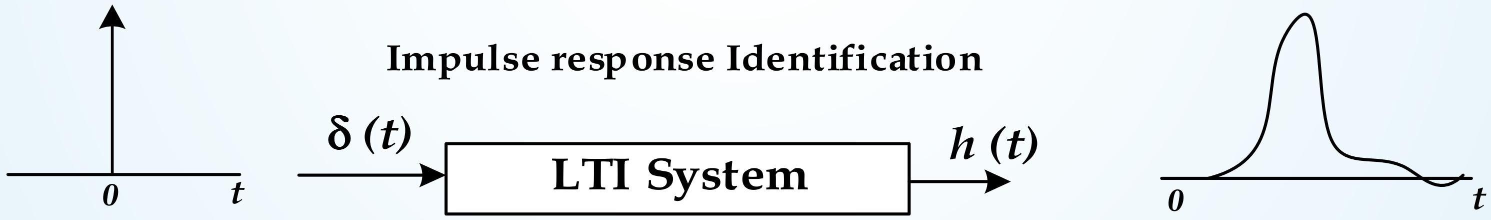
✓ The timing functions, $w_L^n(t)$ and $w_H^n(t)$, are extracted through linear inversion as follows:

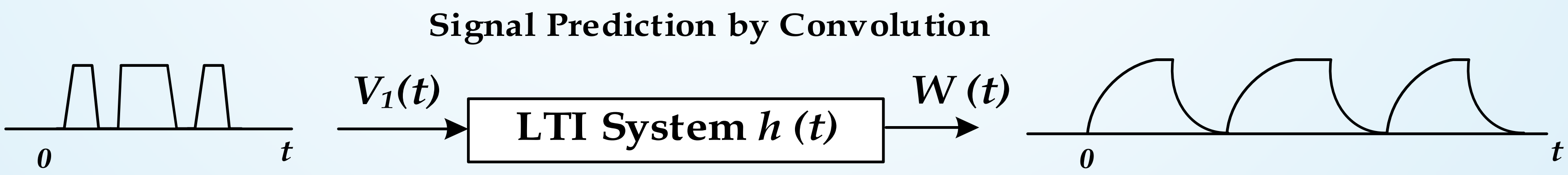
$$\begin{bmatrix} w_L^n(t) \\ w_H^n(t) \end{bmatrix} = \begin{bmatrix} I_{L,b}^n(t) & I_{H,b}^n(t) \\ I_{L,a}^n(t) & I_{H,a}^n(t) \end{bmatrix}^{-1} \cdot \begin{bmatrix} I_{2,a}^n(t) \\ I_{2,b}^n(t) \end{bmatrix}$$

$$; n = r, f$$

FIR FILTER IDENTIFICATION FROM STEP RESPONSE

✓ Assuming that the buffer behaves as a linear time invariant (LTI) system for the rising and falling step transitions.





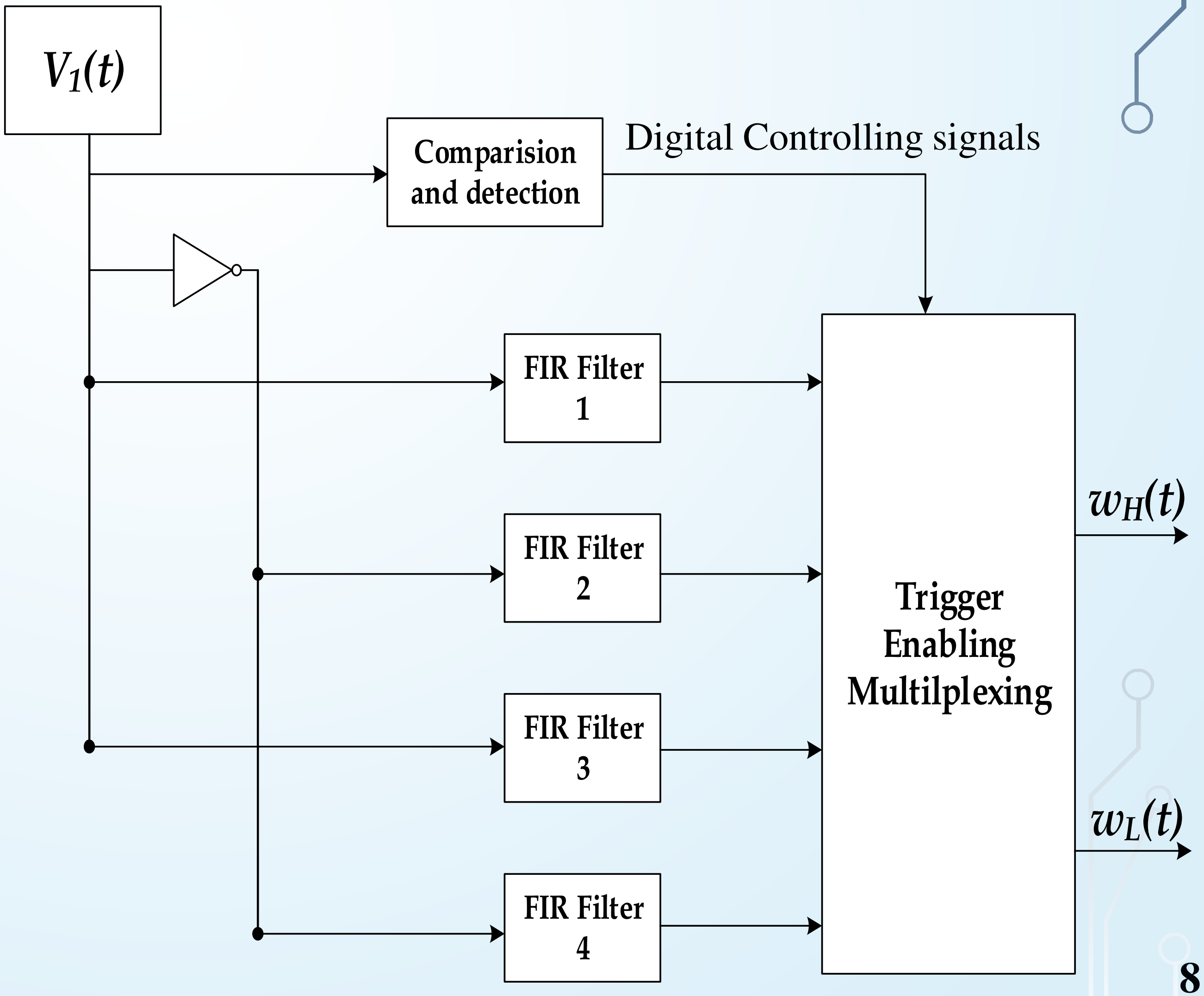
✓ The impulse response h(t) can be represented as the derivative of a step response.

✓ Impulse response estimation :

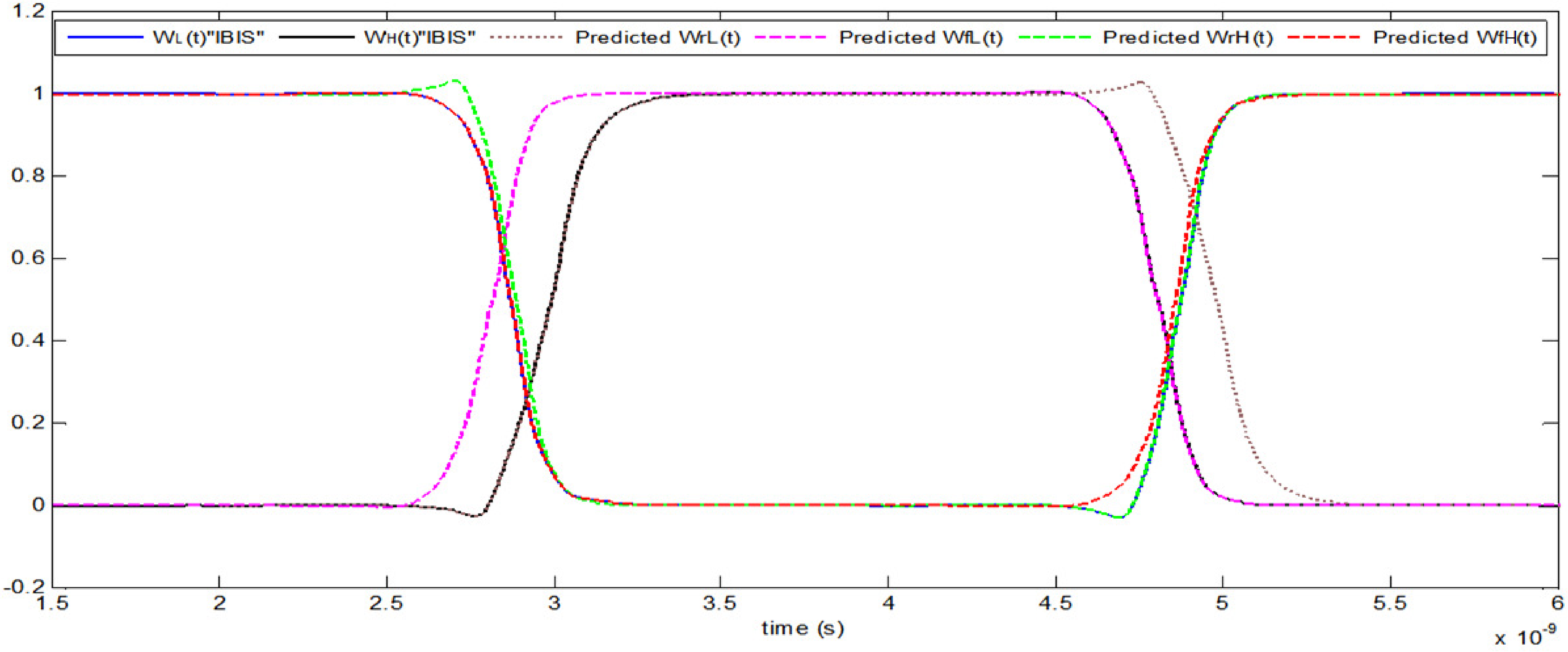
Impulse Input (t) = $V_1(t) - V_1(t-1)$; and Impulse Response(t)=$w_L^n(t) - w_L^n(t-1)$

PRE-DRIVER MODEL IMPLEMENTATION

- ✓ The timing signals W(t) are controlled by the input bit pattern characteristics V1(t).
- ✓ The filter banks capture the dynamics of the rising and falling step transitions.
- ✓ Combinational and sequential digital processing are required to generate the accurate controlling signals,

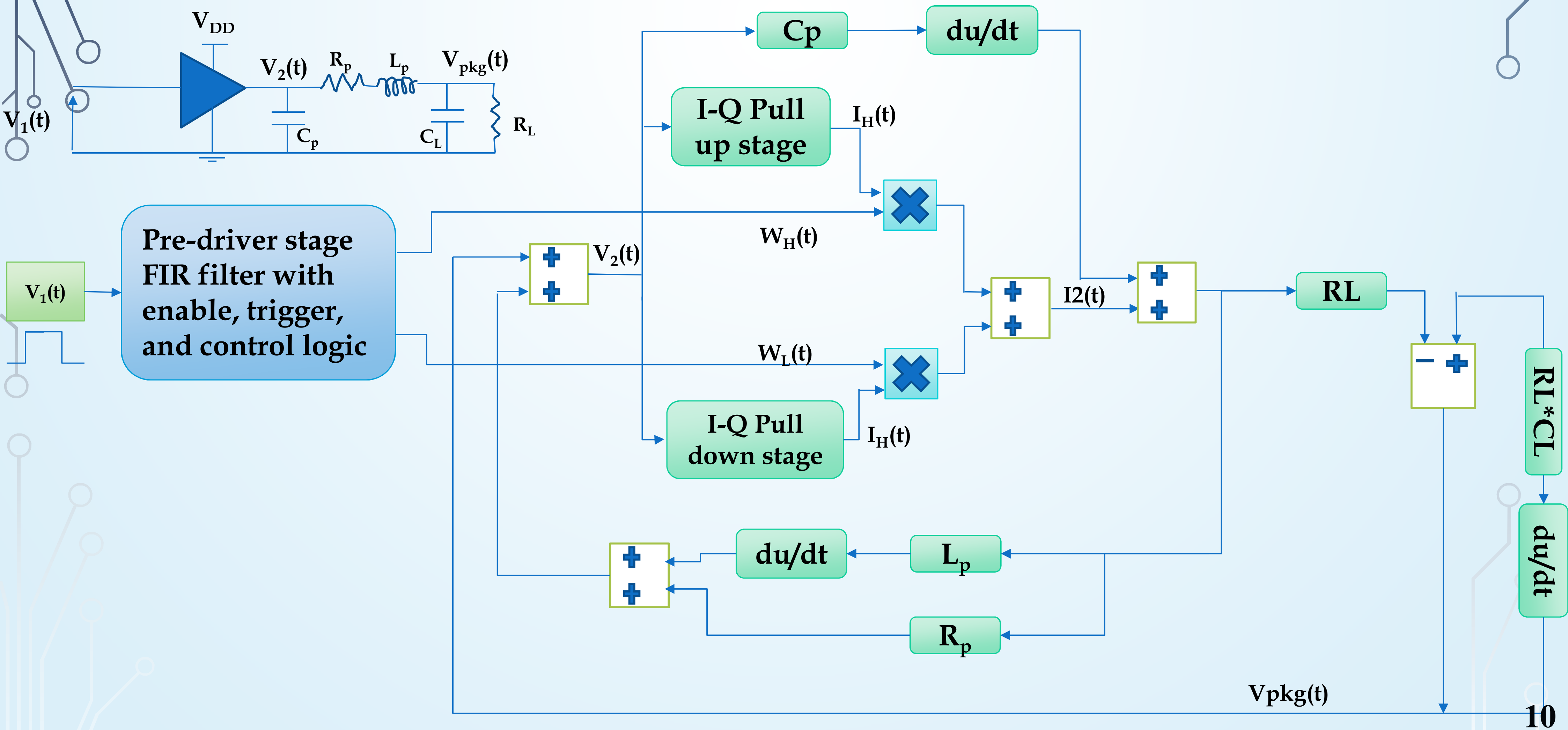


PREDICTED VS IBIS TIMING FUNCTION



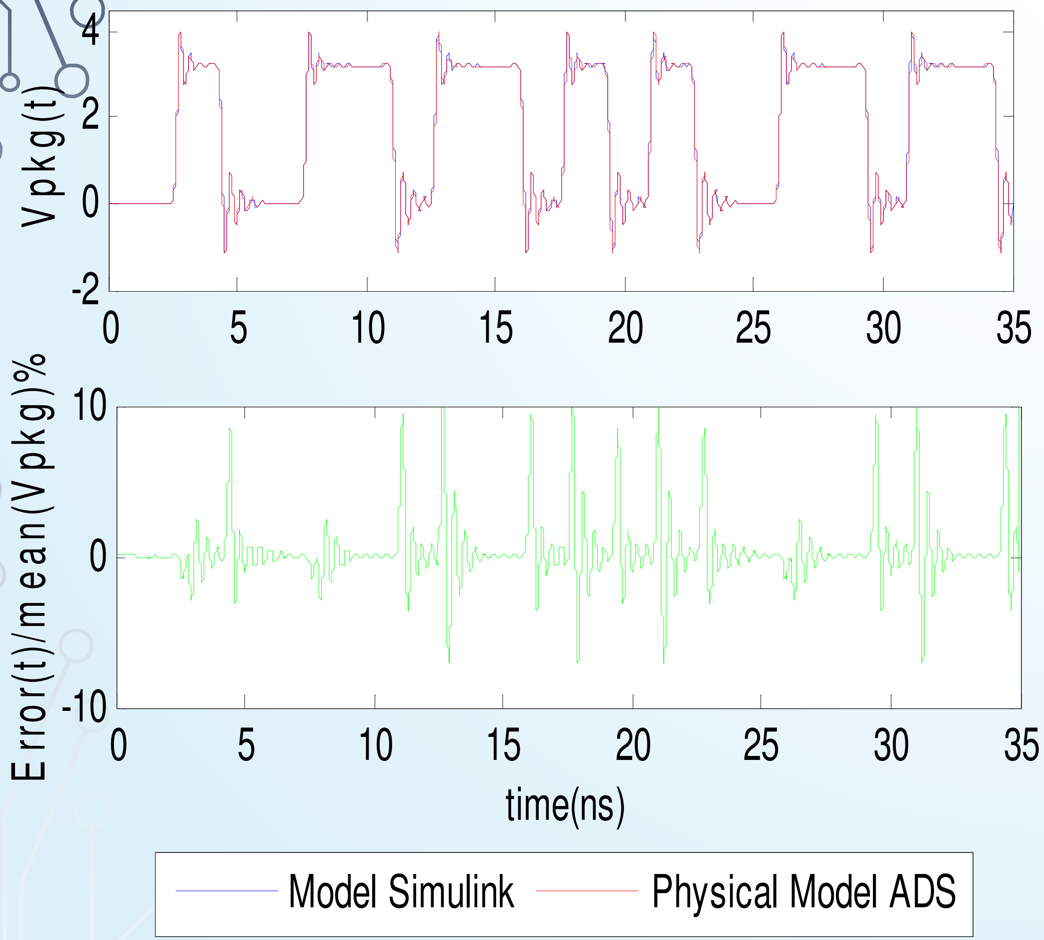
The controlling digital signals are required to multiplex the activation of the signal resulted from the four filters.

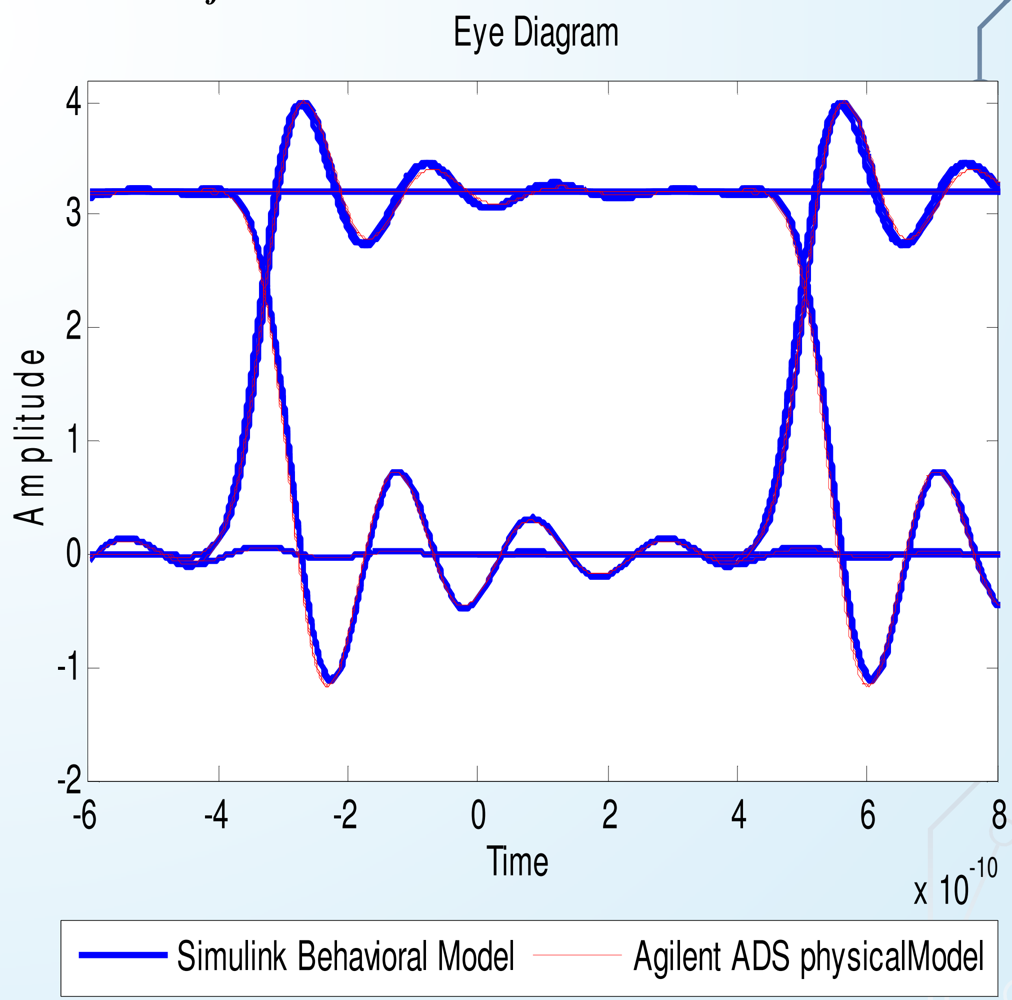
MODEL IMPLEMENTATION IN MATLAB



MIXED-SIGNAL MODEL VALIDATION

***$V_1(t)$* : data rate =600Mbps *t_r=300 ps and t_f* =400ps**





CONCLUSIONS

- ✓ The model's functions, which include the nonlinear conduction (I-V) and displacement (Q-V) characteristics, are extracted from bias-dependent S-parameter data.

- ✓ The pre-driver filters are extracted from observed I/O time domain data.
- ✓ -Combinational and sequential processing is used to implement the conditionally executed subsystems to account for the pre-driver nonlinear dynamics.

- ✓ The measurement-based and table-driven behavioral model from mixed-domain extraction are implemented as LUTs in MATLAB-Simulink software. This presents an alternative solution for the IBIS extraction and the VHDL-AMS implementation.

- ✓ This model is generated for I/O interfaces designed in CMOS bulk technology and the extension of the model formulation is required to account for I/O buffers that are designed based on Fully Depleted Silicon On Insulator (FD-SOI) technology.

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