



IBIS Open Forum Minutes

Meeting Date: **May 10, 2017**

Meeting Location: **SPI-E IBIS Summit, Baveno, Italy**

VOTING MEMBERS AND 2017 PARTICIPANTS

ANSYS	Curtis Clark, Toru Watanabe
Applied Simulation Technology	(Fred Balistreri)
Broadcom	Bob Miller
Cadence Design Systems	Brad Brim, Sivaram Chillarige, Debabrata Das Ambrish Varma
Cisco Systems	(Bidyut Sen)
CST	Stefan Paret*, Matthias Troescher, Burkhard Doliwa* Danilo Di Febo*, Alexander Melkozerov*
Ericsson	Zilwan Mahmod*
GLOBALFOUNDRIES	Steve Parker
Huawei Technologies	(Jinjun Li)
IBM	Luis Armenta, Adge Hawes, Greg Edlund
Infineon Technologies AG	(Christian Sporrer)
Intel Corporation	Michael Mirmak, Hsinho Wu, Eddie Frie Gianni Signorini*, Barry Grquinovic
IO Methodology	Lance Wang
Keysight Technologies	Radek Biernacki, Pegah Alavi, Fangyi Rao Stephen Slater, Jian Yang
Maxim Integrated	Joe Engert, Don Greer, Yan Liang, Hock Seow
Mentor, A Siemens Business (formerly Mentor Graphics)	Arpad Muranyi, Nitin Bhagwath*, Praveen Anmula Fadi Deek, Raj Raghuram, Dmitry Smirnov Bruce Yuan, Carlo Bleu*
Micron Technology	Randy Wolff, Justin Butterfield
Qualcomm	Tim Michalka, Kevin Roselle
Raytheon	Joseph Aday
Signal Integrity Software	Mike LaBonte, Walter Katz, Todd Westerhoff
Synopsys	Kevin Li, Ted Mido, John Ellis, Scott Wedge
Teraspeed Labs	Bob Ross
Xilinx	(Raymond Anderson)
ZTE Corporation	(Shunlin Zhu)
Zuken	Ralf Bruening, Michael Schaeeder*, Alfonso Gambuzza*

OTHER PARTICIPANTS IN 2017

Accton	Raul Lozano
ASUS	Nick Huang, Bin-chyi Tseng
Continental AG	Stefanie Schatt*

eASIC	David Banas
Extreme Networks	Bob Haller
Ghent University	Paolo Manfredi*
Hamburg University of Technology	Torsten Revschel*, Torsen Wendt*
IdemWorks	Michelangelo Bandinu*
Independent	Dian Yang
John Baprawski, Inc.	John Baprawski
KEI Systems	Shinichi Maeda
Lattice Semiconductor	Maryam Shahbazi, Dinh Tran
Leading Edge	Pietro Vergine*
Politecnico di Torino	Claudio Siviero*, Stefano Grivet-Talocia*, Igor Stievano*
SAE International	(Logen Johnson)
Signal Metrics	Ron Olisar
SPISim	Wei-hsing Huang
STMicroelectronics	Fabio Brina*, Olivier Bayet*
Toshiba	Yasuki Torigoshi
Université Blaise Pascal	Mohamed Toure*
Université de Bretagne Occidentale	Mihai Telescu*

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Meeting Number	Meeting Password
May 12, 2017	624 999 876	IBISfriday11

For teleconference dial-in information, use the password at the following website:

<http://tinyurl.com/zeulerr>

All teleconference meetings are 8:00 a.m. to 9:55 a.m. US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting.

NOTE: "AR" = Action Required.

OFFICIAL OPENING

The IBIS Open Forum Summit was held in Baveno, Italy at the Grand Hotel Dino following the 2017 SPI conference. About 23 people representing 15 organizations were recorded in attendance.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

<http://www.ibis.org/summits/may17/>

Michael Schaefer welcomed all attendees. He presented the agenda and sincerely thanked the sponsors ANSYS, CST, Mentor, A Siemens Business, and Zuken. He also expressed gratefulness in the name of the IBIS committee to the SPI 2017 organization team, namely Manuela Trincherio, Stefano Grivet-Talocia and Igor Stievano, and all others for their support.

Following an IBIS summit tradition all attendees were pleased to give a short self-introduction and describe their relationship to IBIS and IBIS-AMI. The audience consisted of IBIS users, tool vendors, and people from universities or institutes. A few of them had no experience with IBIS models thus far.

ACCURATE MACROMODELS OF OUTPUT BUFFERS WITH PRE-/DE-EMPHASIS

Gianni Signorini*, Claudio Siviero**, Igor Simone Stievano**, Stefano Grivet-Talocia**

*Intel Corporation, Germany; **Politecnico di Torino, Italy

[Presented by Gianni Signorini, Intel Corporation, Germany]

Gianni gave a short introduction of IBIS and IBIS-AMI modeling of pseudo and true differential drivers. He explained the elements of an IBIS-AMI model, i.e. analog IBIS, AMI configuration file and EQ in the executable .dll file. Gianni showed a SERDES channel simulation with driver, channel and receiver. He pointed out possible disadvantages of current IBIS (AMI) models:

- TX EQ is assumed to be an ideal FIR filter.
- Simple R+C+Linear slope approximation without frequency dependency.
- AMI covers differential signal only, no common mode signal is included.

Gianni showed details of the Mpilog modeling framework extended to support TX models with pre-/de-emphasis. The models are parametric mathematical representations with parameter values post-processed from SPICE simulations. Output static characteristics are represented by 3D surface models. Pre-/de-emphasis effects are embedded in weighting functions. C_comp is modeled with time-domain vector fitting pole/zero models. The Mpilog model shows outstanding accuracy for both differential and common-mode signals.

An attendee asked if there is any limitation of the IBIS-AMI model at 10GHz. Gianni responded that it depends on the TX and how well the linearity assumption is fulfilled.

COMPACT MULTIVARIATE SURFACE APPROXIMATIONS FOR POWER-AWARE I/O MODELS

Claudio Siviero*, Gianni Signorini**, Stefano Grivet-Talocia*, Igor Simone Stievano*,

*Politecnico di Torino, Italy; **Intel Corporation, Germany

[Presented by Claudio Siviero, Politecnico di Torino, Italy]

Claudio introduced requirements for macromodels for signal and power integrity simulations. Open issues with IBIS power-aware models include modeling of static characteristics,

rising/falling waveforms, and supply current relative to supply voltage as well as power-supply port modeling. He then discussed R&D work being done with Mpilog macromodels for SI and PI simulation. A flexible and modular approach using Mpilog can be implemented in SPICE/Verilog-A. Possible IBIS enhancements were shown to improve power-aware modeling. Validation test showed excellent accuracy in SI/PI co-simulations.

A question was asked if the consideration of ground bounce is possible (regarding slide 3). Claudio responded that in principle it is possible to consider the explicit modeling of the VSS pin as well. However, Gianni Signorini did emphasize that the meaningfulness of such an enhancement is strictly dependent on how the PDN model has been extracted. In fact, very popular extraction tools consider only the current loop between the VDD and VSS planes, so that only the voltage difference between VDD and VSS pins matters. Those are actually the typical case studies the presentation authors concentrated on. On the other hand, there are other extraction tools that account for a third reference plane and consider both the current loop VDD-reference and VSS-reference. In that case the modeling of the VSS pin voltage activity makes sense.

Another question was asked about the performance of the model. Claudio responded that the original IBIS model is only a little bit faster.

IBIS UPDATE

Mike LaBonte, Signal Integrity Software (SiSoft), USA
[Presented by Michael Schaefer, Zuken, Germany]

Michael presented the IBIS roster. Currently IBIS has 25 member companies. He also mentioned the current IBIS officers and referred to the officer's election later in May. He said that only a few people do most of the work and that this is sometimes difficult for them to bring this in line with their job duties. Michael briefly explained how the Open Forum works and the different task groups. He said the IBIS' parent organization is the SAE ITC. He explained that standard changes are requested by BIRDS.

Michael summarized the IBIS history and showed the timeline of IBIS 7.0 which is scheduled for December, 2017. He finally gave a preview of the most likely content. Most important features to come are:

- BIRD 147.6, Back-channel Support
- BIRD 158.5, AMI Ts4file Analog Buffer Models
- BIRD 189.3, Interconnect Modeling Using IBIS-ISS and Touchstone

Someone asked how many BIRDS are active today. Are open BIRDS separately listed on the web page? Michael responded that all BIRDS are listed on the web page including their statuses (open, accepted, rejected). There is no extra list for just open BIRDS (to his knowledge).

INTERCONNECT MODELING USING IBIS-ISS AND TOUCHSTONE

Michael Mirmak, Intel Corporation, USA
[Presented by Stefan Paret, CST AG, Germany]

Stefan stated that BIRD189.x was recently released by the Interconnect Task Group and is

awaiting approval. The BIRD is intended for IBIS Version 7.0, and its purpose is to improve package and on-die interconnect models by supporting IBIS-ISS and Touchstone models. This includes models of both I/O and supply connections. An optional die pad interface between pins and buffers is introduced. A one-to-one path connection is assumed for I/Os. Supply rails can have multiple terminals and be merged at the various interfaces. Stefan showed some details of new keywords and subparameters as well as syntax examples.

IBIS EXTENSIONS FOR TURN-AROUND CYCLE SIMULATIONS

Nitin Bhagwath*, Arpad Muranyi*, Randy Wolff**

*Mentor, A Siemens Business, USA; **Micron Technology, USA

[presented by Nitin Bhagwath, Mentor, A Siemens Business, USA]

Nitin noted there is a need to simulate turn around cycles on memory busses because of SI effects that can negatively affect read/write or write/read transitions. Simulating bus turnaround is desirable with IBIS models. He showed what is currently missing in IBIS to correctly model transitions from 1 -> High Z , High Z -> 1, 0 -> High Z , High Z -> 0. He also mentioned that information of ODT activation behavior is needed. Nitin showed how this extra information can be fitted into IBIS, e.g. new tables for transition waveforms and a Bus_hold Submodel for smoothly turning on/off ODT. A simple change to the Bus_hold Submodel type would allow the Submodel to be triggered by a digital control signal from the EDA tool instead of from a voltage waveform crossing event.

He showed a correlation with SPICE (good agreement) and pointed out that behavioral modeling is needed for this to avoid long simulations runs (> 1 hour vs. < 1 minute). The team working on this is aiming for an IBIS BIRD to make turn-around cycle simulations possible with IBIS models. Additional modeling challenges include modeling of bus transitions between multiple on-die termination settings.

A statement from the audience was that this type of simulation is needed.

An additional comment was that this approach considers the output signal only. Should this also take power noise into account (power awareness)? Nitin responded that this is a good point. He will have to look onto this.

CONCLUDING ITEMS

Michael Schaefer again thanked the sponsors ANSYS, CST, Mentor, A Siemens Business, and Zuken, the presenters, organizers and attendees.

The meeting concluded at approximately 5:00 PM.

NEXT MEETING

The next IBIS Open Forum teleconference meeting will be held May 12, 2017. Votes on BIRD158.5 and BIRD186.3 are scheduled. Votes on conducting IBIS Summits at EDI CON and EPEPS also are scheduled.

The following IBIS Open Forum teleconference meeting is tentatively scheduled on June 2, 2017.

NOTES

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This meeting was conducted in accordance with ANSI guidance.

All inquiries may be sent to info@ibis.org. Examples of inquiries are:

- To obtain general information about IBIS.
- To ask specific questions for individual response.
- To subscribe to the official ibis@freelists.org and/or ibis-users@freelists.org email lists (formerly ibis@eda.org and ibis-users@eda.org).
- To subscribe to one of the task group email lists: ibis-macro@freelists.org, ibis-interconn@freelists.org, or ibis-quality@freelists.org.
- To inquire about joining the IBIS Open Forum as a voting Member.
- To purchase a license for the IBIS parser source code.
- To report bugs or request enhancements to the free software tools: ibischk6, tschk2, icmchk1, s2ibis, s2ibis2 and s2iplt.

The BUG Report Form for ibischk resides along with reported BUGs at:

<http://www.ibis.org/bugs/ibischk/>
<http://www.ibis.org/bugs/ibischk/bugform.txt>

The BUG Report Form for tschk2 resides along with reported BUGs at:

<http://www.ibis.org/bugs/tschk/>
<http://www.ibis.org/bugs/tschk/bugform.txt>

The BUG Report Form for icmchk resides along with reported BUGs at:

<http://www.ibis.org/bugs/icmchk/>
http://www.ibis.org/bugs/icmchk/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

<http://www.ibis.org/bugs/s2ibis/bugs2i.txt>
<http://www.ibis.org/bugs/s2ibis2/bugs2i2.txt>
<http://www.ibis.org/bugs/s2iplt/bugspl.txt>

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

<http://www.ibis.org/>

Check the IBIS file directory on ibis.org for more information on previous discussions and results:

<http://www.ibis.org/directory.html>

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SAE STANDARDS BALLOT VOTING STATUS

Organization	Interest Category	Standards Ballot Voting Status	March 10, 2017	March 31, 2017	April 21, 2017	May 10, 2017
ANSYS	User	Active	X	X	X	-
Applied Simulation Technology	User	Inactive	-	-	-	-
Broadcom Ltd.	Producer	Inactive	X	-	X	-
Cadence Design Systems	User	Active	X	X	X	-
Cisco Systems	User	Inactive	-	-	-	-
CST	User	Inactive	-	-	-	X
Ericsson	Producer	Inactive	-	-	-	X
GLOBALFOUNDRIES	Producer	Active	X	-	X	-
Huawei Technologies	Producer	Inactive	-	-	-	-
IBM	Producer	Active	X	X	X	-
Infineon Technologies AG	Producer	Inactive	-	-	-	-
Intel Corp.	Producer	Active	X	X	X	X
IO Methodology	User	Active	X	X	X	-
Keysight Technologies	User	Active	X	X	X	-
Maxim Integrated	Producer	Inactive	-	-	-	-
Mentor, A Siemens Business	User	Active	X	X	X	X
Micron Technology	Producer	Active	X	X	X	-
Qualcomm	Producer	Inactive	-	-	-	-
Raytheon	User	Inactive	-	-	-	-
Signal Integrity Software	User	Active	X	X	X	-
Synopsys	User	Active	X	X	X	-
Teraspeed Labs	General Interest	Active	X	X	X	-
Xilinx	Producer	Inactive	-	-	-	-
ZTE	User	Inactive	-	-	-	-
Zuken	User	Inactive	-	-	-	X

Criteria for SAE member in good standing:

- Must attend two consecutive meetings to establish voting membership
- Membership dues current
- Must not miss two consecutive meetings

Interest categories associated with SAE standards ballot voting are:

- Users - members that utilize electronic equipment to provide services to an end user.
- Producers - members that supply electronic equipment.
- General Interest - members are neither producers nor users. This category includes, but is not limited to, government, regulatory agencies (state and federal), researchers, other organizations and associations, and/or consumers.