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Variability-Aware Modeling of Supply Induced Jitter in CMOS Inverters

by

Vinod Kumar Verma and Jai Narayan Tripathi

Dept. of Electrical Engineering,
Indian Institute of Technology Jodhpur,
India

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Outline

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Introduction

- At nano-scale technology a larger number of transistors are integrated per unit area of silicon.
- **Low-power, multifunctional** and **compact consumer electronics devices.**
- Variability is a big concern for the designers due to multiple factors.
- Electrical performance of ICs is mainly affected by two factors.
  - **Environmental and functional factor:** supply fluctuation, temperature, and switching activity of the transistors.
  - **Physical limitations (inaccuracies during fabrication process):** variation in oxide thickness, length and width of the transistors, variation in electrical properties of interconnects, etc.

- A. Chandrakasan, W. J. Bowhill, and F. Fox, *Models of Process Variations in Device and Interconnect*, 2001, pp. 98–115.
- S. K. Saha, "Compact MOSFET Modeling for Process Variability-Aware VLSI Circuit Design," *in IEEE Access*, vol. 2, pp. 104-115, 2014.

Introduction

- Because of the variations in these parameters the signal gets affected.
- Several issues related to signal and power integrity arise such as: **variation in rise/fall time i.e. time interval error (TIE) and jitter**.
- **TIE** is a short term variations of a transition edge of signal with respect to its ideal position in time.
- Difference between the maximum and the minimum value of TIE determines **Jitter**.

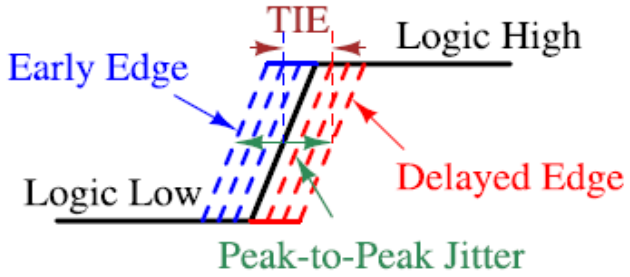


Fig. 1: TIE and Jitter Representation

- A. Chordia and J. N. Tripathi, "Uncertainty quantification of RF circuits using stochastic collocation techniques," *IEEE Electromagnetic Compatibility Magazine*, vol. 11, no. 1, pp. 45–56, 2022.
- J. N. Tripathi, V. K. Sharma and H. Shrimali, "A Review on Power Supply Induced Jitter," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 9, no. 3, pp. 511-524, March 2019, doi: 10.1109/TCPMT.2018.2872608.

Problem Statement

- **IC ALD1105** having monolithic dual N-channel and P-channel complimentary matched transistor pair.
- Input data rate 1 Mbps is taken.
- The output response of 120 CMOS inverters are taken without inserting any noise.
- No single inverter is precisely similar to the others.
- Variation in the output response spans up to 25 nsec at $V_{DD}/_2$ level.

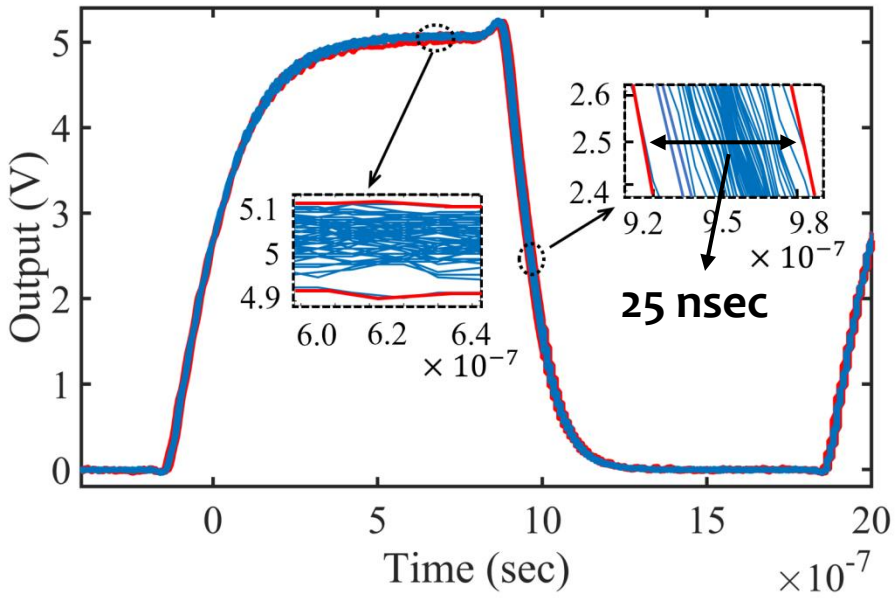


Fig. 2: Output responses of 120 CMOS inverters.

Problem Statement

- CMOS inverter is one of the fundamental building blocks in ICs.
- Its timing uncertainty may affect performance the entire system.
- In high-speed VLSI designs, it is essential to understand the impact of jitter on the performance of the system.
- This work studies the effect of **variability on PSIJ**.
- **Variability aware modeling of Jitter** can be helpful for VLSI designers to optimize their design for better performance.

- **Noise:** A small signal noise source is inserted at the supply terminal.

$$v_s(t) = A_s \sin(\omega_s t + \emptyset_s)$$

- **Input Data Signal:** A fast rising edge of the input signal is considered with rise time τ.

$$V_{in}(t) = \begin{cases} 0, & if\ t \le 0 \\ V_{DD}\left(\frac{t}{\tau}\right), & if\ 0 \le t \le \tau \\ V_{DD}, & if\ t \ge \tau \end{cases}$$

- **Process Parameters subjected to Random Variations:** Width of the transistors ($\boldsymbol{W_P}$ and $\boldsymbol{W_N}$) are considered as random variable.

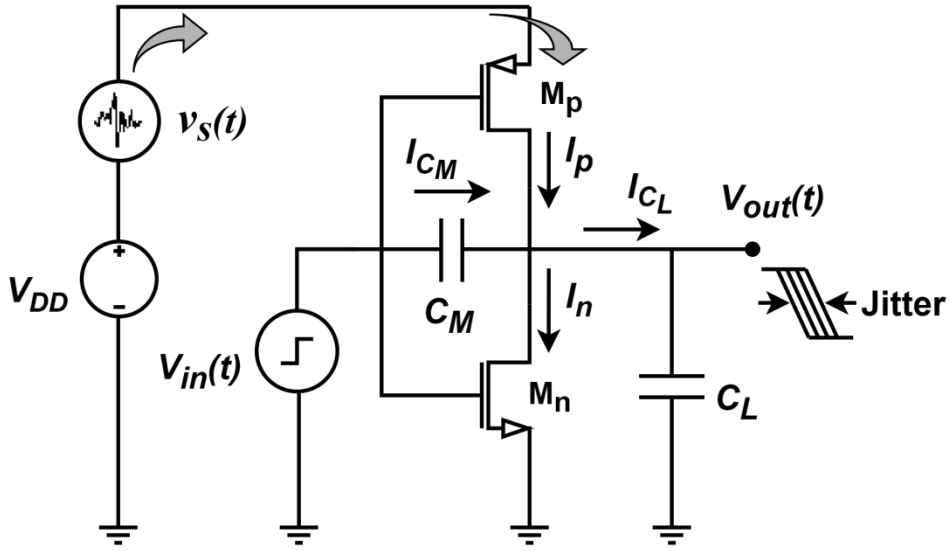


Fig. 3: CMOS Inverter in the presence of PSN.

Note: *Random variables are represented in bold letters.*

Input-Output Relationship

- The entire falling edge of the output is divided in to **5 regions** depending on the operating mode of the transistors.

	Mode of Operation of Transistors	Range of Input (Voltage levels)	Duration of the Time of various Regions
I.	M_P: Linear, M_N: Cut-off	0 to V_{TN}	0 to $T_1 = \frac{V_{TN}\tau}{V_{DD}}$
II.	M_P: Linear M_N: Enters in Saturation	V_{TN} to $(V_{DD} - \lvert V_{TP}\rvert)$	T_1 to $T_2 = \frac{(V_{DD}-V_{TP})\tau}{V_{DD}}$
III.	M_P: Enters in Cut-off M_N: Saturation	$V_{DD} - \lvert V_{TP}\rvert$ to V_{DD}	T_2 to $T_3 = \tau$
IV.	M_P: Cut-off M_N: Saturation	V_{DD}	T_3 to $T_4 = T_{sat_n}$
V.	M_P: Cut-off, M_N: Linear	V_{DD}	T_4 to ∞

- The output response of every region is concatenated in time to obtain the final output response.

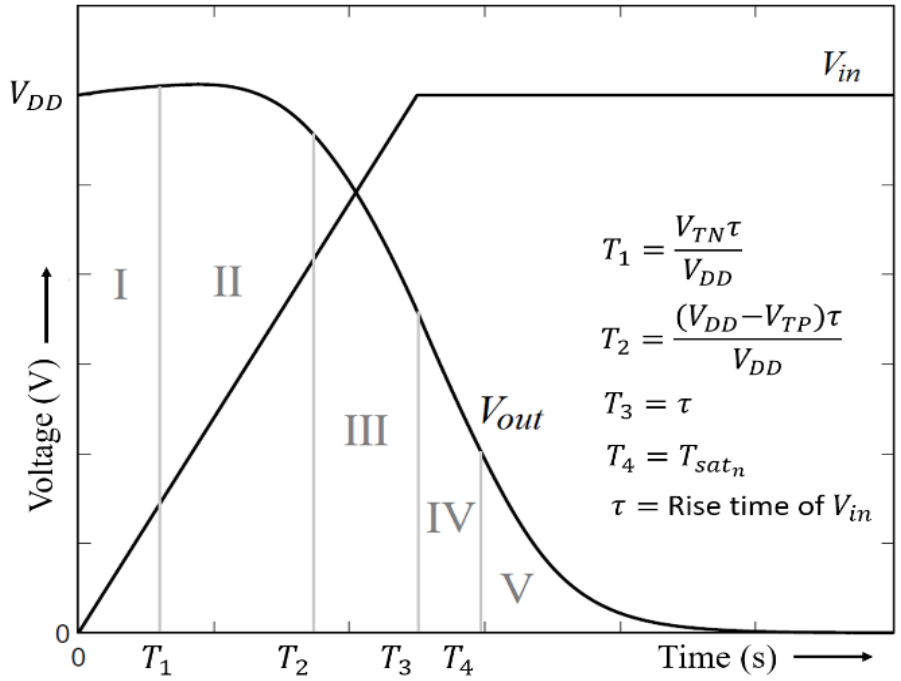


Fig. 4: Output Response of CMOS Inverter for rising input.

- V. K. Verma and J. N. Tripathi, "Analytical Modeling of Deterministic Jitter in CMOS Inverters," in *IEEE Transactions on Signal and Power Integrity*, doi: 10.1109/TSIPI.2023.3264961.
- V. K. Verma and J. N. Tripathi, "Device parameters based analytical modeling of ground-bounce induced jitter in cmos inverters," *IEEE Transactions on Electron Devices*, vol. 69, no. 10, pp. 5462–5469, 2022

Input-Output Relationship

- Estimation of **jitter** needs to done at midpoint (i.e. $V_{DD}/_2$ voltage level) of the output response i.e. in Region-4.
- Output Response of Region-4:

$$\boldsymbol{V_{out}(t)} = \boldsymbol{V_{34}} - \frac{\boldsymbol{\gamma_3}}{2}(V_{DD} - V_{TN})^2(t - T_3)$$

- $\boldsymbol{V_{34}}$ is a constant term used to maintain the continuity between the Region-3 and Region-4.

$$\boldsymbol{V_{34}} = \frac{\gamma_1 V_{DD}}{\tau}(T_3 - T_2) + \frac{\boldsymbol{\gamma_3}\tau}{3V_{DD}}\left[\frac{V_{DD}}{\tau}(T_3 - T_2) - V_{TN}\right]^3 + \boldsymbol{V_{23}}$$

where,

$$\gamma_1 = \frac{C_M}{C_M + C_L}, \boldsymbol{\gamma_3} = \frac{\boldsymbol{\beta_n}}{(1+\delta_n)(C_M + C_L)}, \boldsymbol{\beta_n} = \mu_n C_{ox}\frac{\boldsymbol{W_n}}{L_n}$$

Modeling of Jitter with Variability

- Suppose ϕ_{s_0} is the initial phase of the noise source, the phase value for j^{th} edge is:

$$\phi_{s_j} = \phi_{s_0} + \omega_s T_d (j-1)$$

- The output expression for j^{th} transition edge can be given as:

$$\boldsymbol{V_{out}(t,j)} = \boldsymbol{V_{34_j}} - \frac{\boldsymbol{\gamma_3}}{2}(V_{DD} - V_{TN})^2 (t - T_3)$$

- The time stamp of the j^{th} transition edge at ${}^{V_{DD}}/_{2}$ voltage level is:

$$\boldsymbol{t_j} = \frac{\boldsymbol{V_{34_j}} - (V_{DD}/2)}{(\boldsymbol{\gamma_3}/2)(V_{DD} - V_{TN})^2} + T_3$$

- Time Interval Error is: $\boldsymbol{TIE_j} = \boldsymbol{t_j} - T_0$

- Jitter at the output is : $\boldsymbol{Jitter} = max(\boldsymbol{TIE_j}) - min(\boldsymbol{TIE_j})$

Results

- **Example-1:** Jitter is estimated only considering **PSN** (amplitude of 40 mV and frequency of 537 MHz).

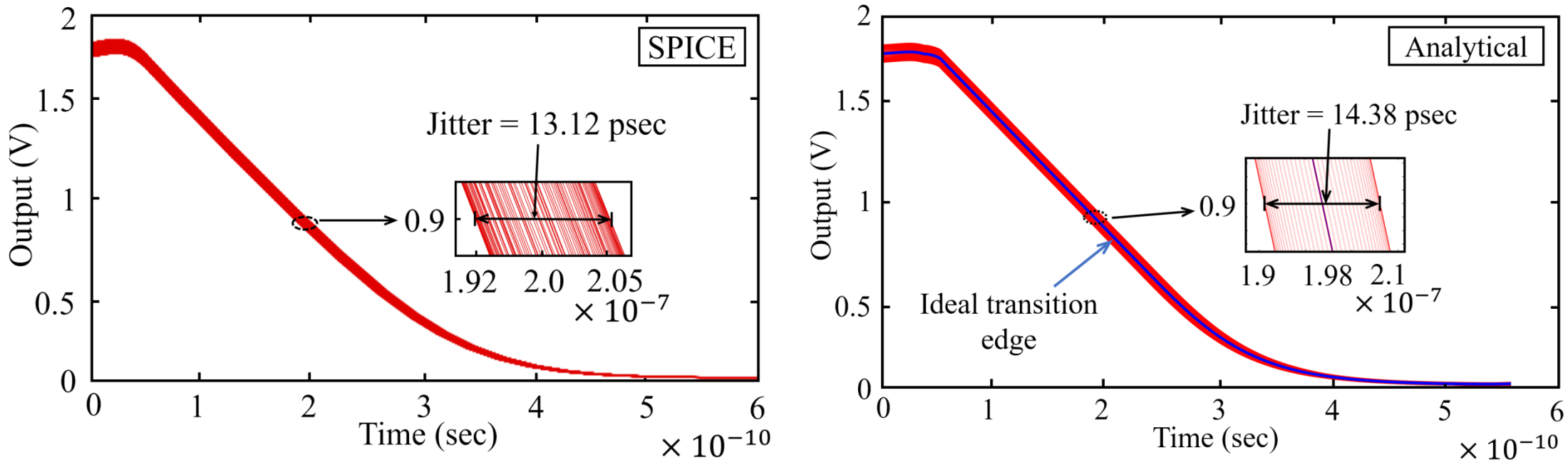


Fig. 5: Output Response of CMOS Inverter in presence of PSN.

Results

- **Example-2:** Jitter is estimated considering random variation in widths of the transistors ($\boldsymbol{W_P}$ and $\boldsymbol{W_N}$) and PSN (amplitude of 40 mV and frequency of 537 MHz).
- 500 samples of each random variables ($\boldsymbol{W_P}$ and $\boldsymbol{W_N}$) are taken.

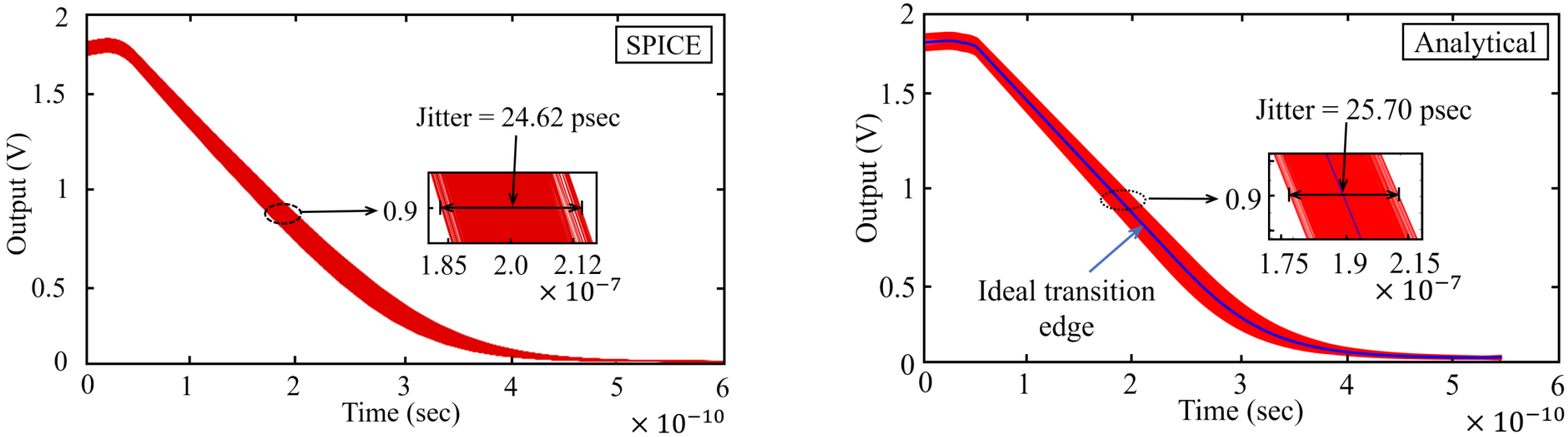
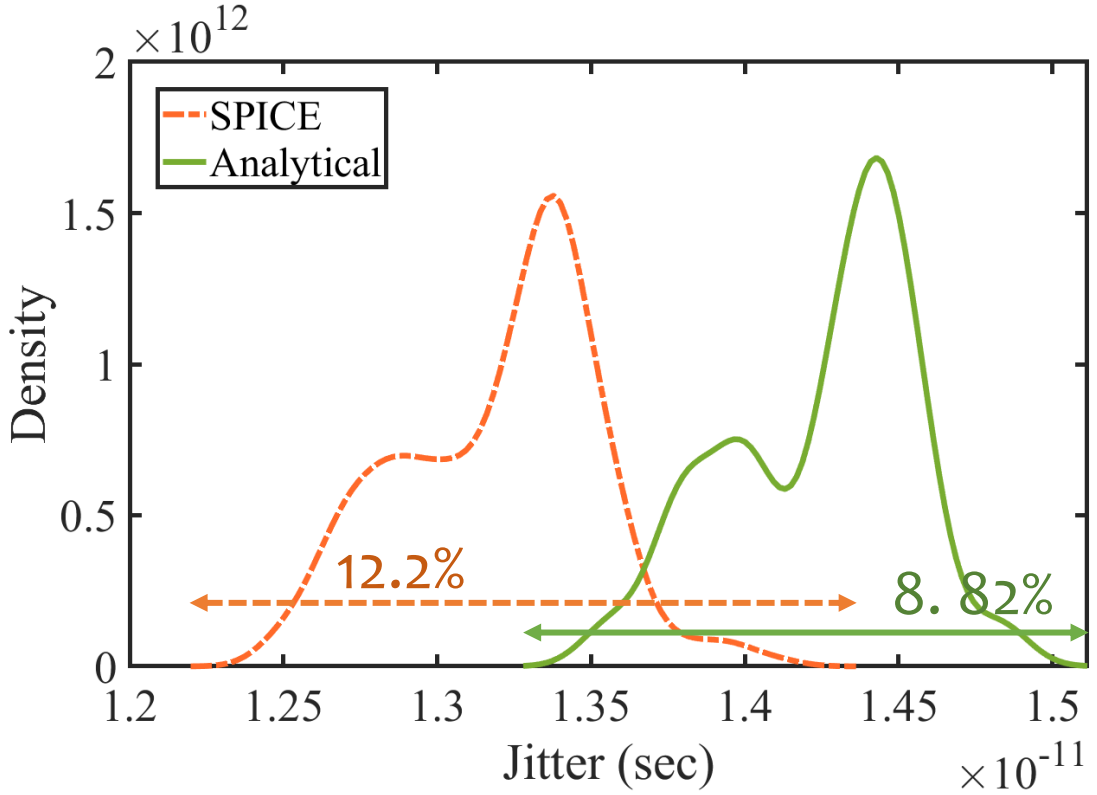


Fig. 6: Output Response of CMOS Inverter in presence of PSN and variability.

Results

- **Example-3:** Jitter is estimated considering random variation in width of the transistors (W_P and W_N) and **PSN** (amplitude of 40 mV and frequency of 537 MHz).
- 900 samples of each random variables (W_P and W_N) are taken.



Statistical Parameters		
Parameters	**SPICE**	**Analytical**
Mean (psec)	13.20	14.24
Standard Deviation (psec)	0.317	0.299
CPU time in hours	2.15	0.36

Fig. 7: Output Response of CMOS Inverter in presence of PSN and variability.

Results

- **Example-4:** The measurement setup was prepared to analyse variation in jitter due to PSN and variability.
- **120 inverters** are designed using **IC ALD1105.**
- UB Jitter = 19.20 nsec, LB Jitter = 20 nsec and Total Jitter = 58.0 nsec.
- $V_{DD} = 5\ V$, Input data rate = 1 Mbps.

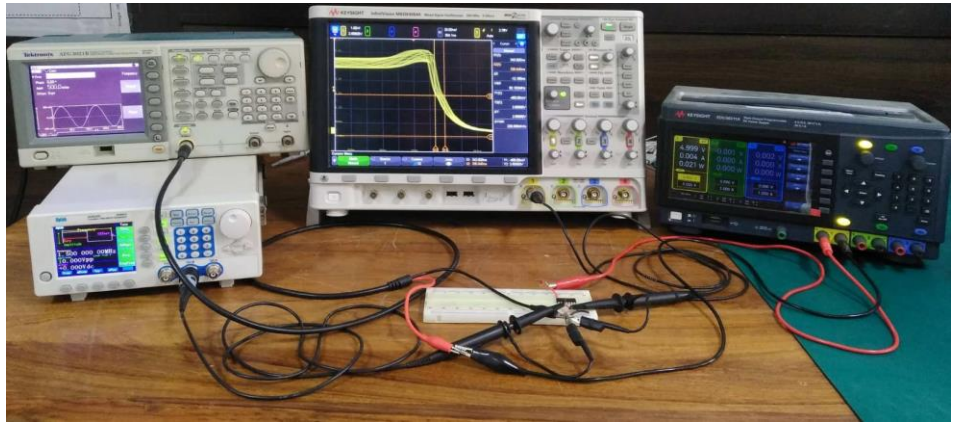


Fig. 8: Measurement setup.

- **PSN:** sinusoidal having peak-to-peak amplitude of 500 mV, and frequency of 4.733 MHz.

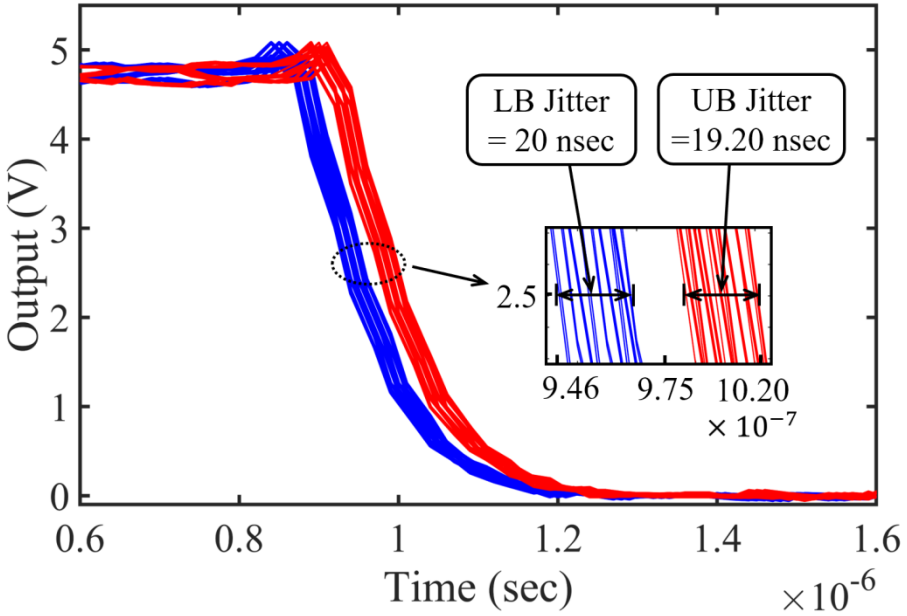


Fig. 9: UB and LB Jitter.

Conclusion

- This work introduces a **new perspective for jitter estimation** in high-speed VLSI circuits.
- It develops an analytical approach to estimate the jitter in CMOS inverters, induced due to power supply noise when process variations are present in the circuit.
- The results suggest that variability-aware modeling of power supply induced jitter in ICs needs to done in order to achieve robust design.
- Overall, variability aware modeling of jitter is can a important tool for VLSI designers.
- It can ensure the better performance of ICs and meet the required design specifications.

THANK YOU