Board-only Power Deliver Prediction for Voltage regulator and Mother Board Designs

Intel Corporation
Data Center Platform Application Engineering
November 15, 2011

Asian IBIS Summit
Shanghai, China

Jiangqi He
Y.L. Li

Legal Disclaimer

Notice: This document contains information on products in the design phase of development. The information here is subject to change without notice. Do not finalize a design with this information. Contact your local Intel sales office or your distributor to obtain the latest specification before placing your product order.

This document contains information on methods under development, is subject to change without notice, and may not reflect the best practices for all participants. Check with your equipment vendor for the latest information on best practices for their equipment. Ultimate responsibility for measurement accuracy lies with those performing measurements, and their methods should be properly evaluated for accuracy.

All products, dates, and figures are preliminary for planning purposes and are subject to change without notice.

Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them.

Copies of documents which have an order number and are referenced in this document, or other Intel literature may be obtained by calling 1-800-548-4725 or by visiting Intel's website at http://www.intel.com.

Agenda

- Introduction
- Simplified SPICE Model
- Case Study and Its Application
- Validation
- Summary and Next Steps

Agenda

- ✓ Introduction
- Simplified SPICE Model
- Case Study & Its Application
- Validation
- Summary & Next Steps

Introduction

Power delivery performance prediction typically is using full wave solvers to extract board, socket, package, and on-chip interconnect. There are many tools and approaches across industries.

However, this typical approach is usually focusing on high frequency noise, involving many piece of software and has certain limitations:

- Very high frequency oriented analysis. Typically looking for many 100s MHz or GHz range
- Extracted full wave S parameters needs macro-modeling for transient analysis
- All full wave solvers has accuracy limitation at low frequency and board analysis needs very accurate low frequency prediction
- Full wave extraction and its associated analysis do not have full explicit information on return path (GND) which is critically important for board design and optimizations.
- Typically full wave approach takes much more time to complete an analysis cycle and also needs electro-magnetics background for many uncertain scenarios during modeling/sims
- Due to its complexity, some OEM/ODM skip prediction step and go directly for testing vehicles
- Therefore, a method that involves less steps, easy to understand, good low frequency accuracy and high efficiency is highly desired!

Introduction (cont'd)

A new methodology is called 'Simplified SPICE Model'. It allows companies to conduct simulations focused on the follows:

- Determine # of MB layers and stack-up
- Choose MB cap types, numbers and locations
- Check the coupling noise due to imperfect common ground
- Validate MB and VR performance in early development stage
- Reduce design cycle time due to faster simulations
- A lot more accurate at low frequency regions.
- Explicitly know exactly return currents
- Least software involvement
- An entry engineer can conduct modeling/simulations

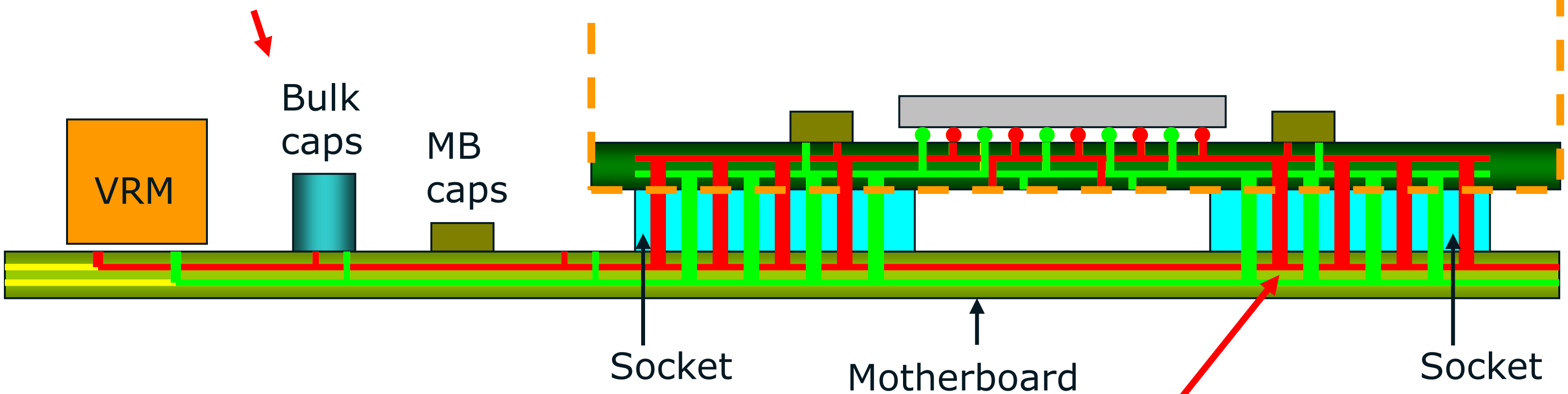
Agenda

- Introduction
- ✓ Simplified SPICE Model
- Case Study and Its Application
- Validation
- Summary and Next Steps

A Typical Network for MB Power Delivery Analysis

MB R network start from VR output Buck Cap

Use Icc / Isa / Itt current Models to replace Die+package models and represent VRTT



MB R network end at Socket pins

Conventional PD Models :
Die (on-die caps) + Package(with caps) + socket + MB + MB/Bulk caps + VR

Simplified SPICE Model for OEMs/ODMs:
VRTT (Icc/Isa/Itt) + socket + MB + MB/Bulk Caps + VR

Simplified SPICE Model Workflow

Step 1. Create MB model

- Create R-network using EDA tool.
- Set up port locations for cap terminations and Vcore, Vsa, Vtt, and socket locations.

Step 2. Socket model

- Get socket pin map from supplier.
- Get R & L values of each socket pin from supplier.
- Group socket pins and scale R & L values.

Step 3. Icc, Isa, Itt models

- Get I (t) model from supplier

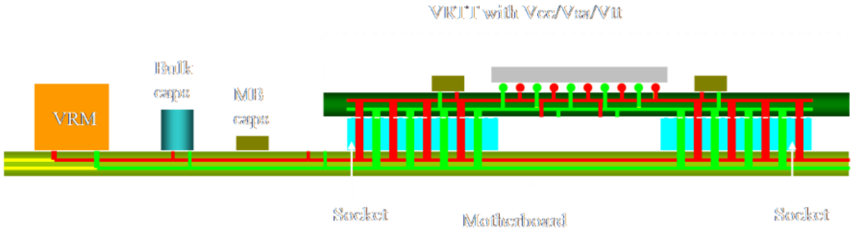
Step 4. VR model

- Use simple VR model from supplier.

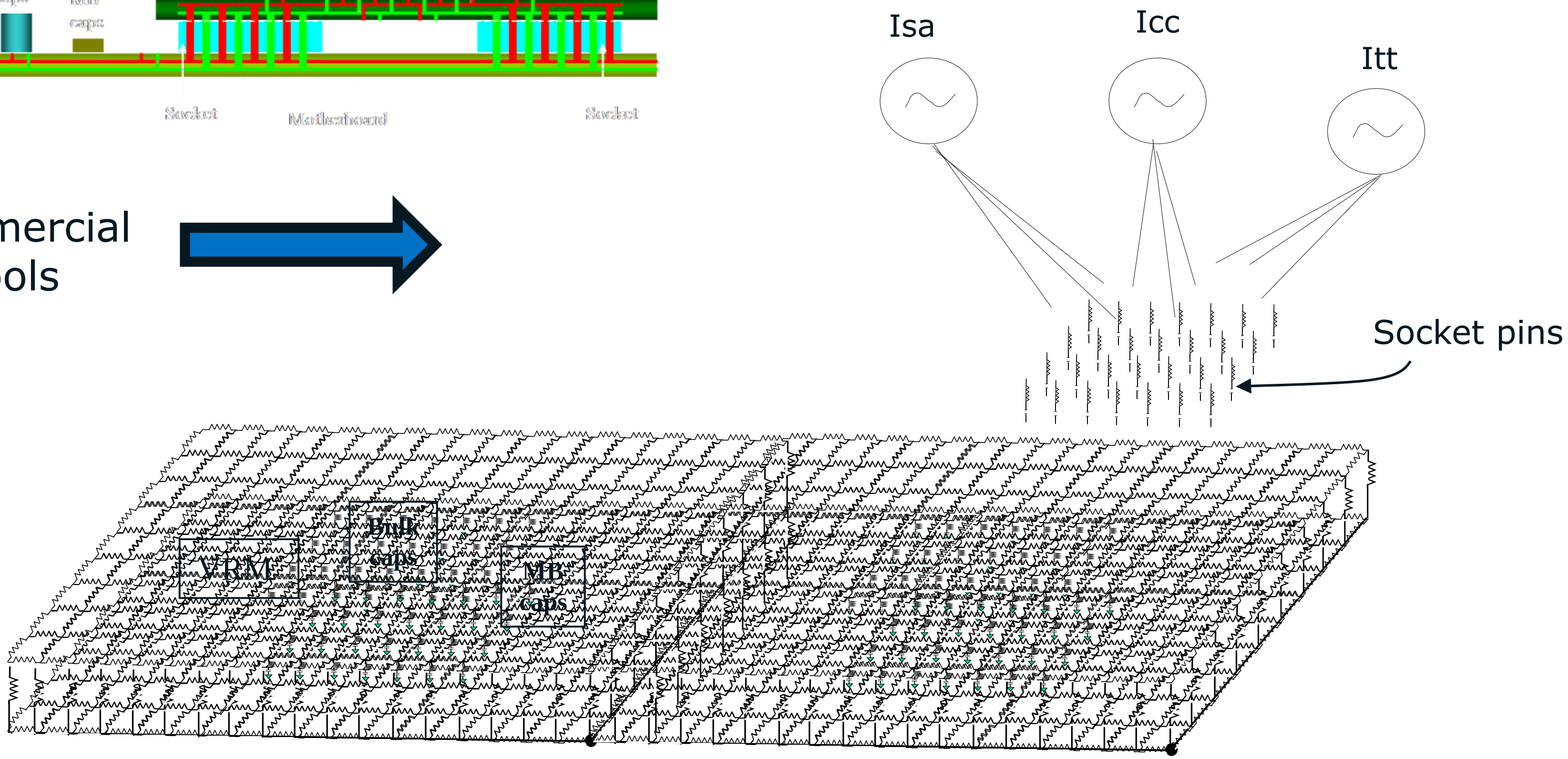
Step 5. Connect all models together and run transient simulations

- Vcore(t), Vsa(t), Vtt(t) separately

Step 6. Compare V(t) with DC and Transient Requirements



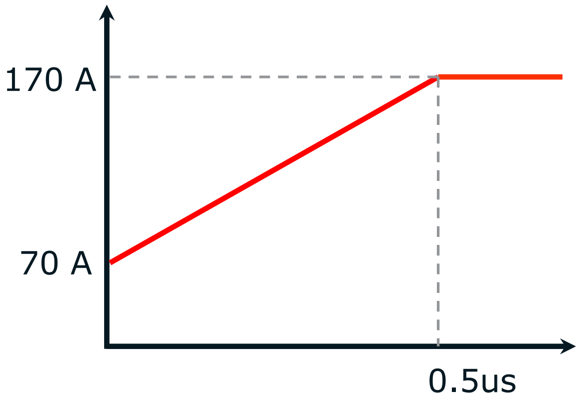
Commercial tools



For VR design: we'll provide current models of Vcore, Vsa, and Vtt and indicate the locations of the socket pins to connect your MB. MB models will only include R from Power/Ground planes and vias.

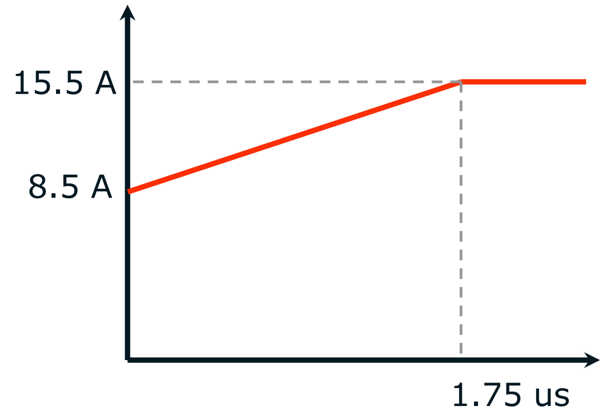
I(t) Models of Vcc/Vsa/Vtt

A server CPU
150 W PVCCP (8 core)



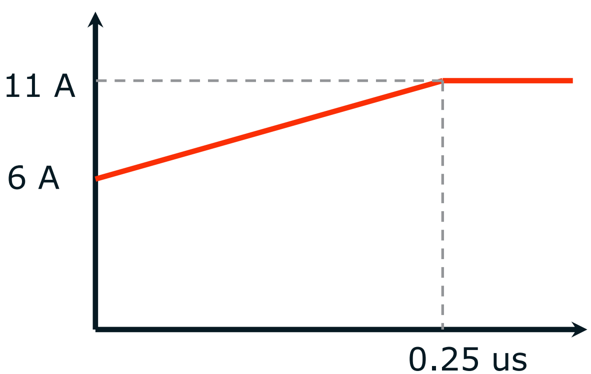
Max step load size = 100 A
Max step load slew rate di/dt ≤ 200 A/μs

A server CPU PVSA



Max step load size = 7A (Current pulse duration <1μs)
Max step load slew rate di/dt ≤ 4.0 A/μs

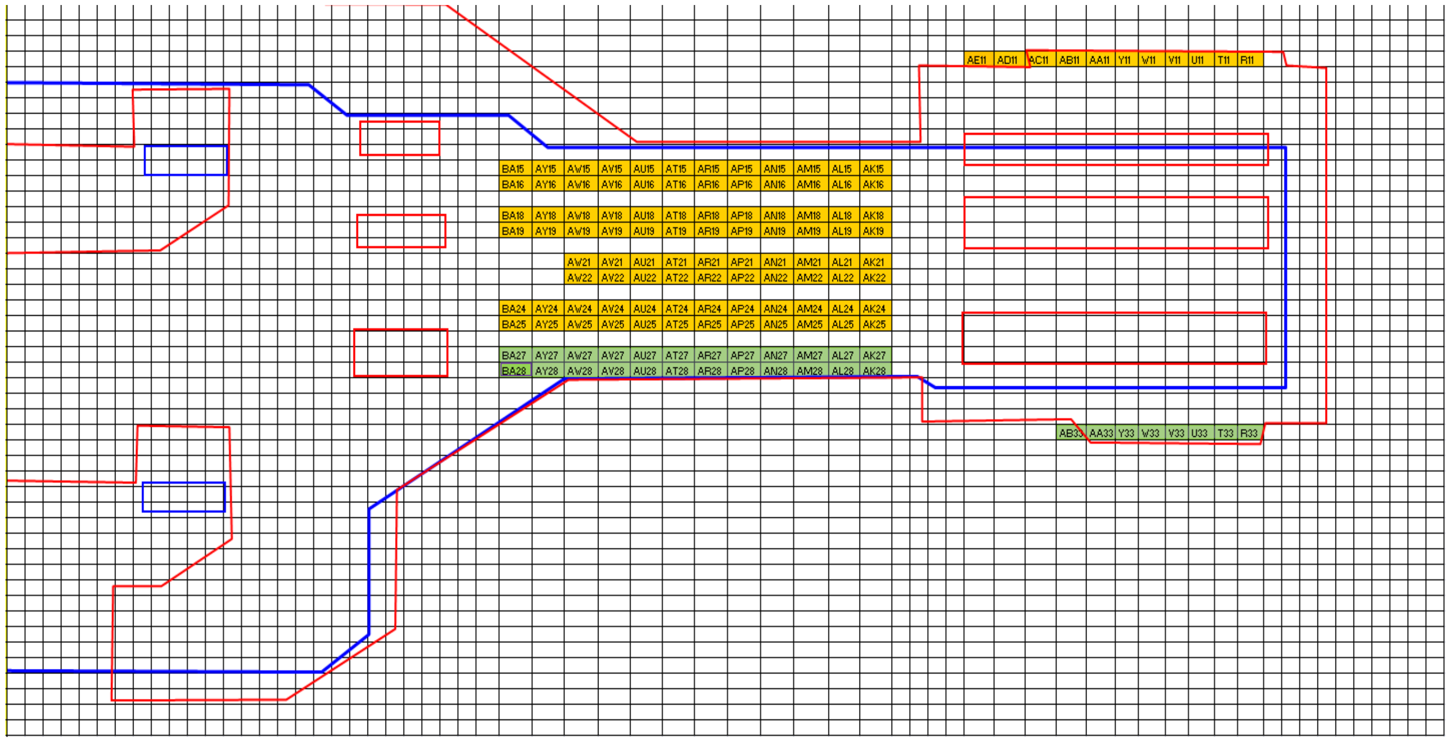
A server CPU PVTT



Max step load size = 5 A
Max step load slew rate di/dt = 20 A/μs

Socket Connections (Top MB Layer, 1 of 5)

MB nodes	PKG nodes
VCCU pins	
AB33	bx11y20
AA33	bx11y21
Y33	bx11y22
W33	bx11y23
V33	bx11y24
U33	bx11y25
T33	bx11y26
R33	bx11y27
BA28	bx16y1
AY28	bx16y2
AW28	bx16y3
AV28	bx16y4
AU28	bx16y5
AT28	bx16y6
AR28	bx16y7
AP28	bx16y8
AN28	bx16y9
AM28	bx16y10
AL28	bx16y11
AK28	bx16y12
BA27	bx17y1
AY27	bx17y2
AW27	bx17y3
AV27	bx17y4
AU27	bx17y5
AT27	bx17y6
AR27	bx17y7
AP27	bx17y8
AN27	bx17y9
AM27	bx17y10
AL27	bx17y11
AK27	bx17y12



You may need to lump several pins as one node.

Stackup (6 layer)

Layer Name	Plane Description	Layer Thickness (mil)	Copper Weight (oz)	Dielectric (eR)	tand (max)
	solder mask	0.50		3.8	0.022
Signal 1	SIGNAL	1.90	1.5		
	prepreg and/or Core	2.70		4.0	0.022
Plane 2	GND	1.30	1.0		
	Prepreg	4.00		4.1	0.022
Signal 3	SIGNAL	1.30	1.0		
	core	39.00		4.0	0.022
Signal 4	SIGNAL	1.30	1.0		
	Prepreg	4.00		4.1	0.022
Plane 5	GND / VDD	1.30	1.0		
	prepreg and/or Core	2.70		4.0	0.022
Signal 6	SIGNAL	1.90	1.5		
	solder mask	0.50		3.8	0.022
	Total	62.40	(+8/-5)		

You may want to get MB resistivity value from MB suppliers.

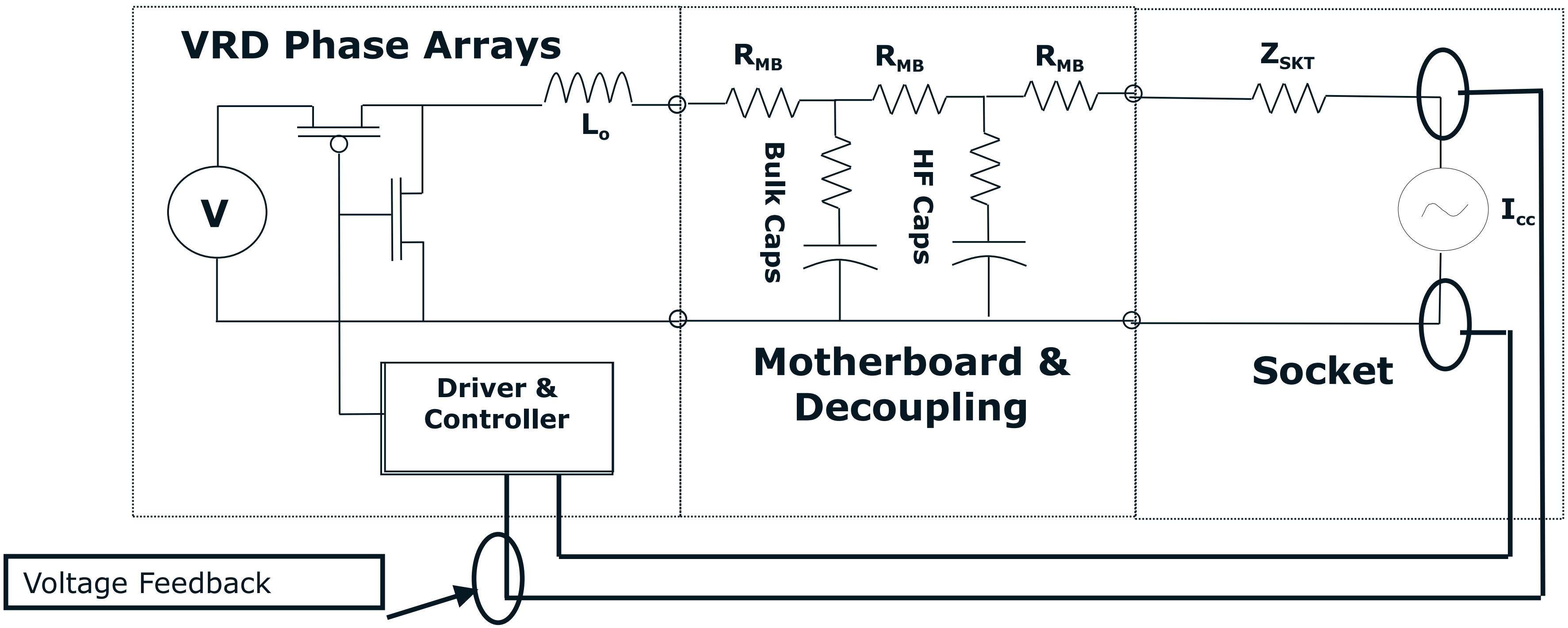
Simplified SPICE Model

Simplified Multiphase VRD (P1~P4) with Socket LoadLine

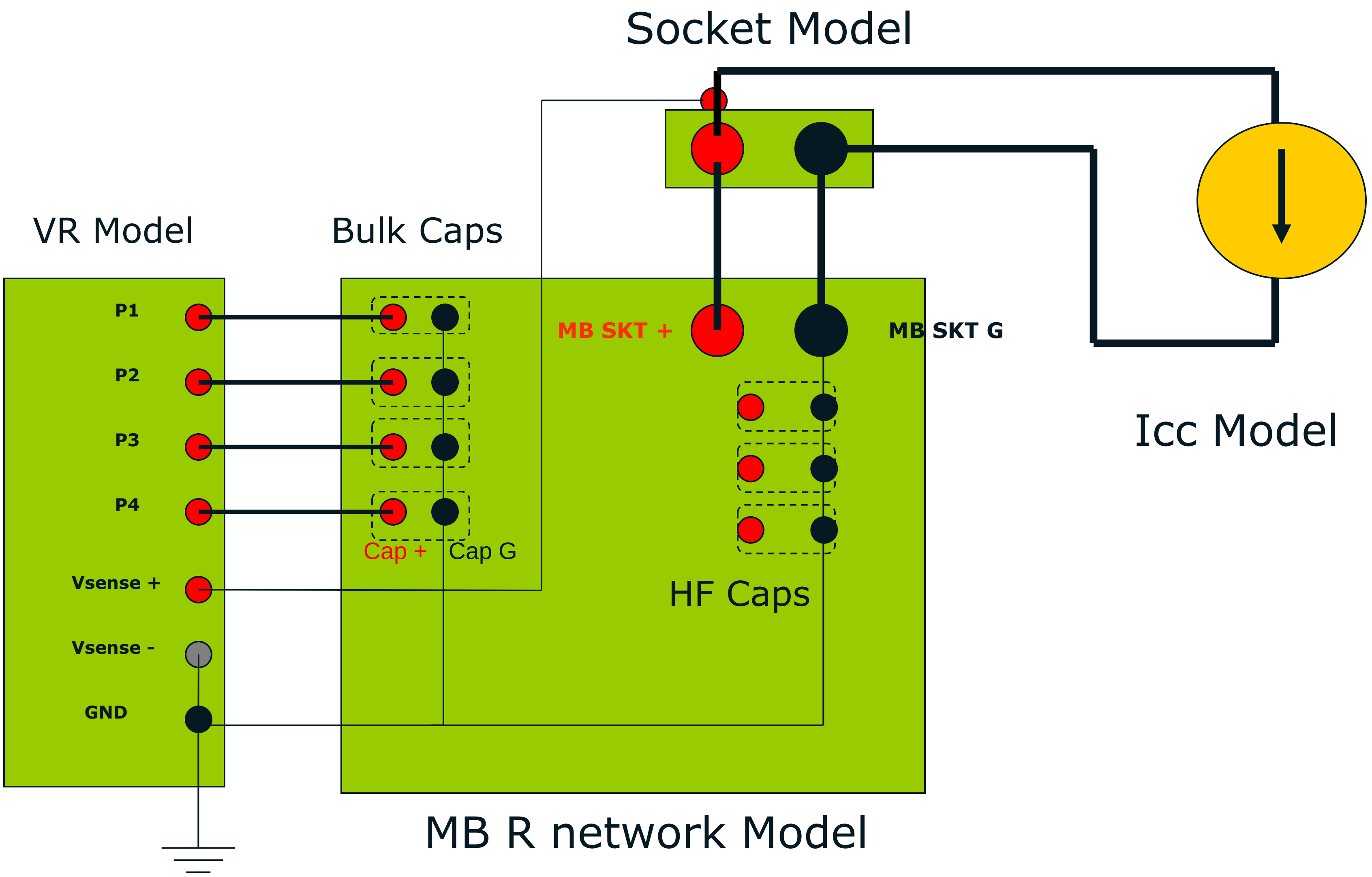
Simplified MB R network include Bulk Caps & Decoupling HF Caps

Icc / Isa / Itt current SPICE Model

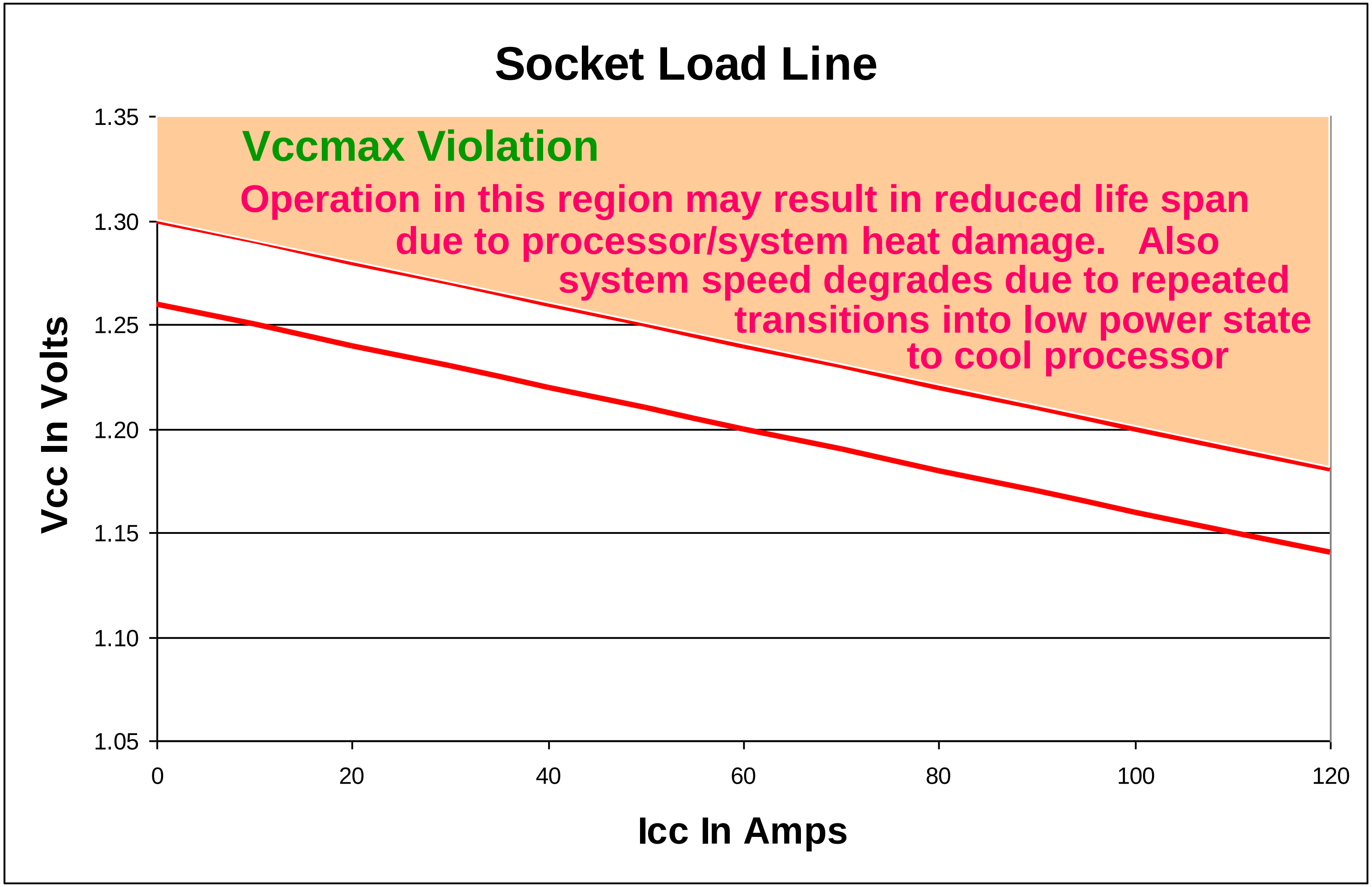
Sensing at CPU Socket



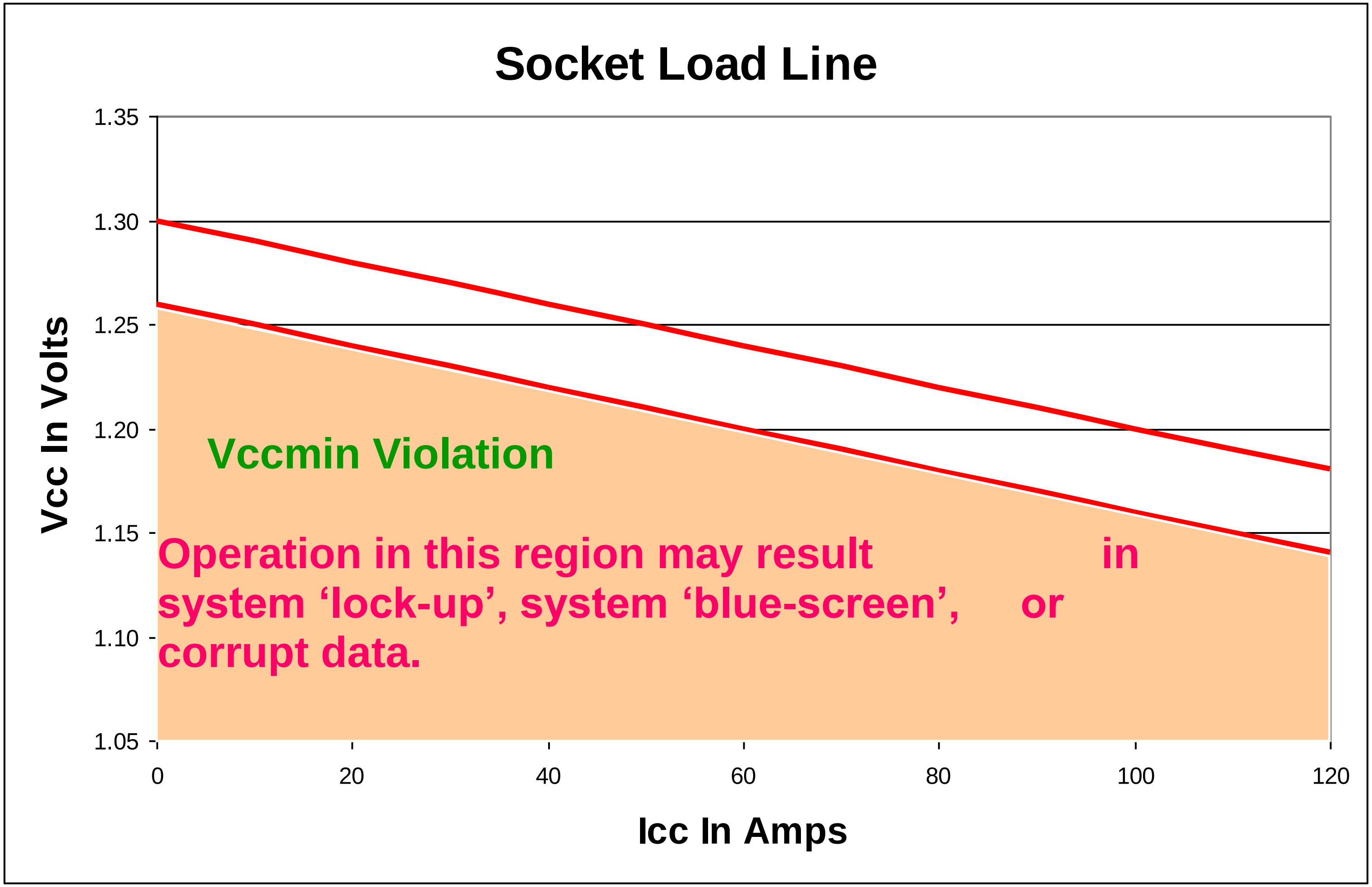
SPICE Model Connection Block Diagram



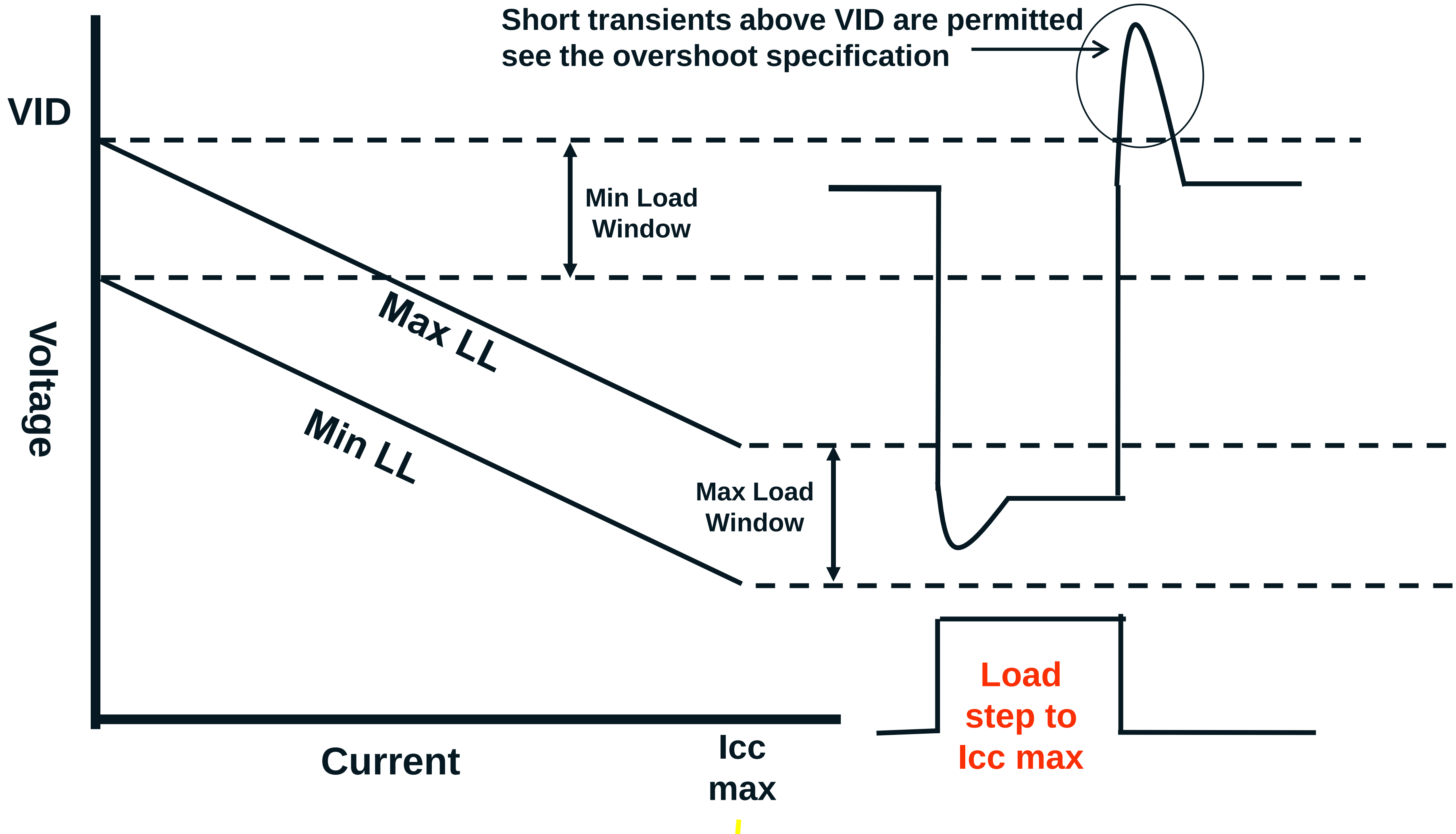
DC Requirements



DC Requirements (cont'd)



Dynamic or Transient Requirements

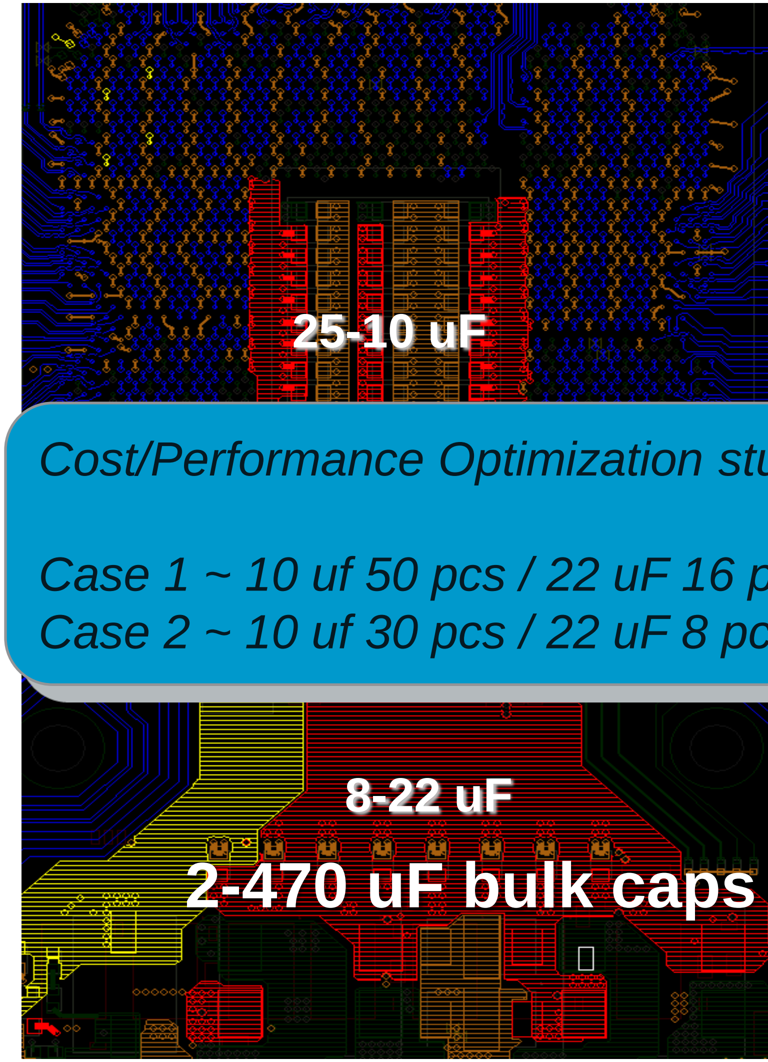


Agenda

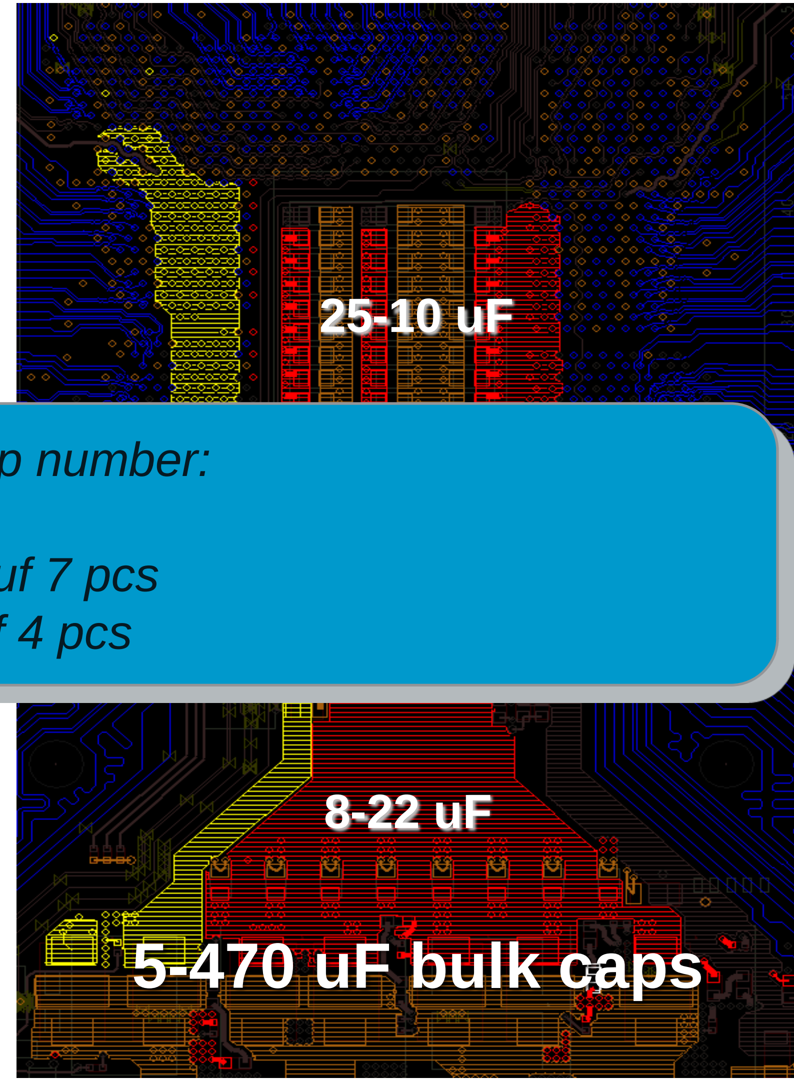
- Introduction
- Simplified SPICE Model
- ✓ Case Study and Its Application
- Validation
- Summary & Next Steps

Case Study –
Cost/Performance Optimization of Cap number

Top caps



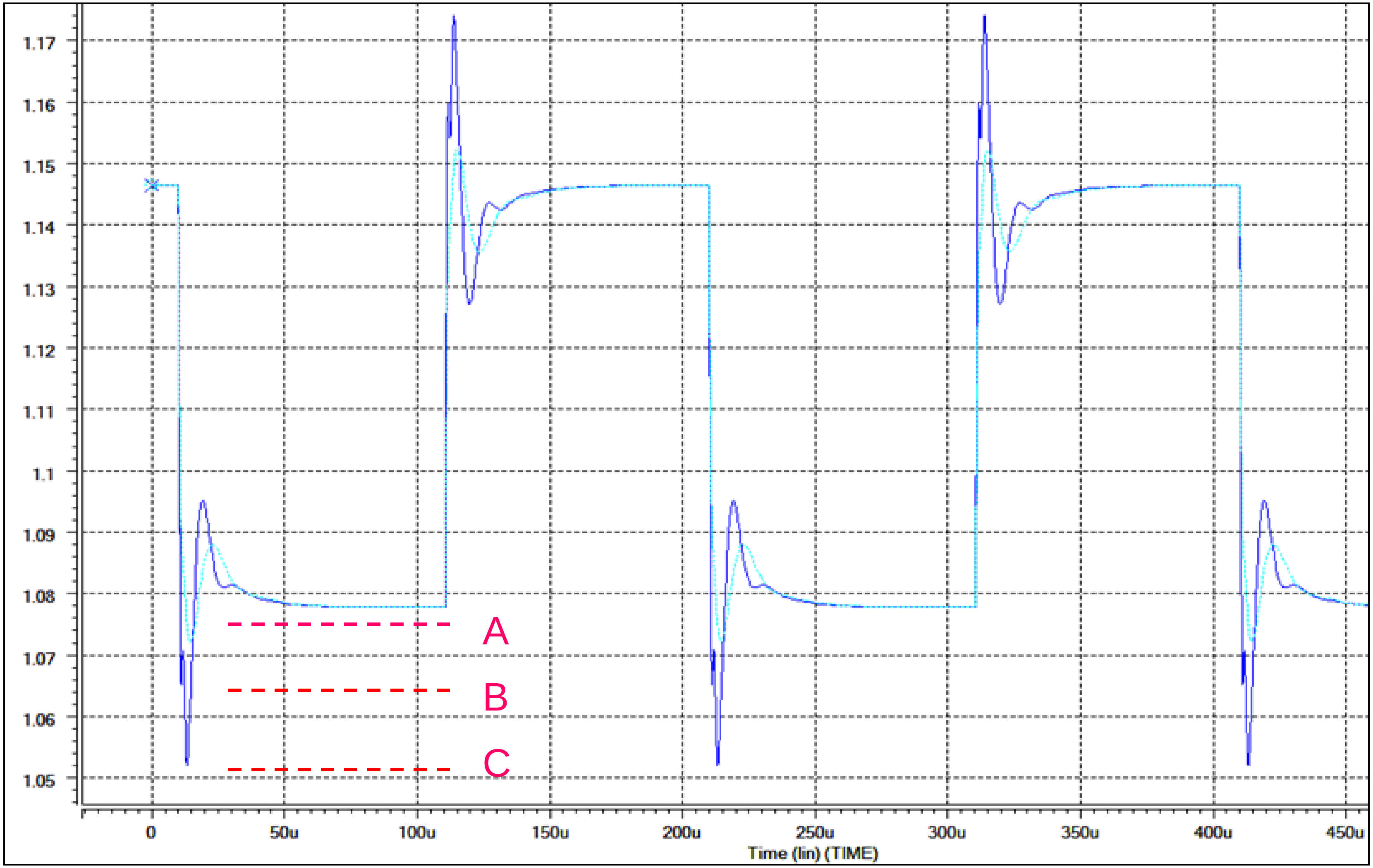
Bottom caps



Cost/Performance Optimization study of Cap number:

Case 1 ~ 10 uf 50 pcs / 22 uF 16 pcs / 470 uf 7 pcs
Case 2 ~ 10 uf 30 pcs / 22 uF 8 pcs / 470 uf 4 pcs

Case Study – *Cost/Performance Optimization of Cap number*



If transient design target is A, both Cases 1 and 2 fail.
If transient design target is B, Case 1 is fine but Case 2 fail.
If transient design target is C, both Cases 1 and 2 are fine.

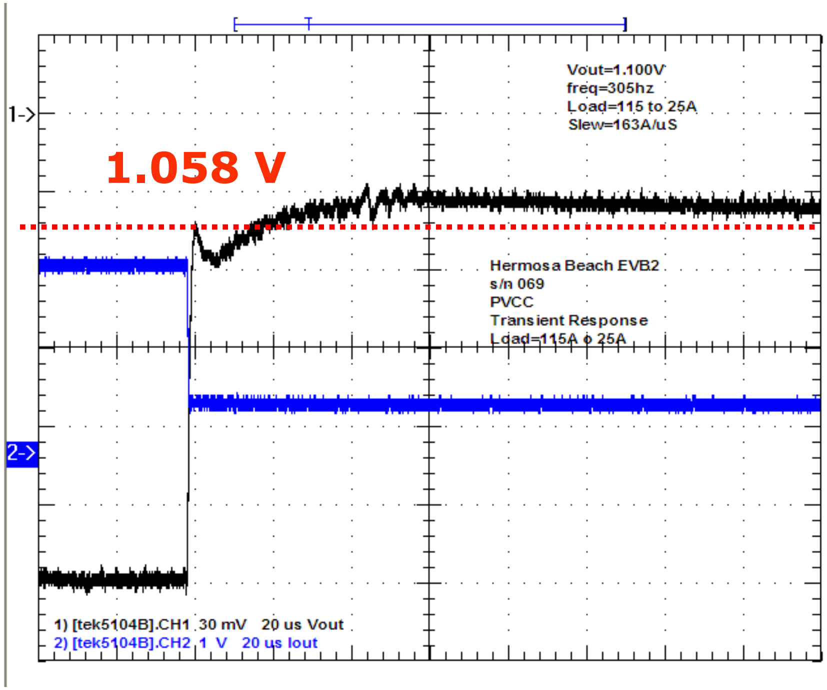
Agenda

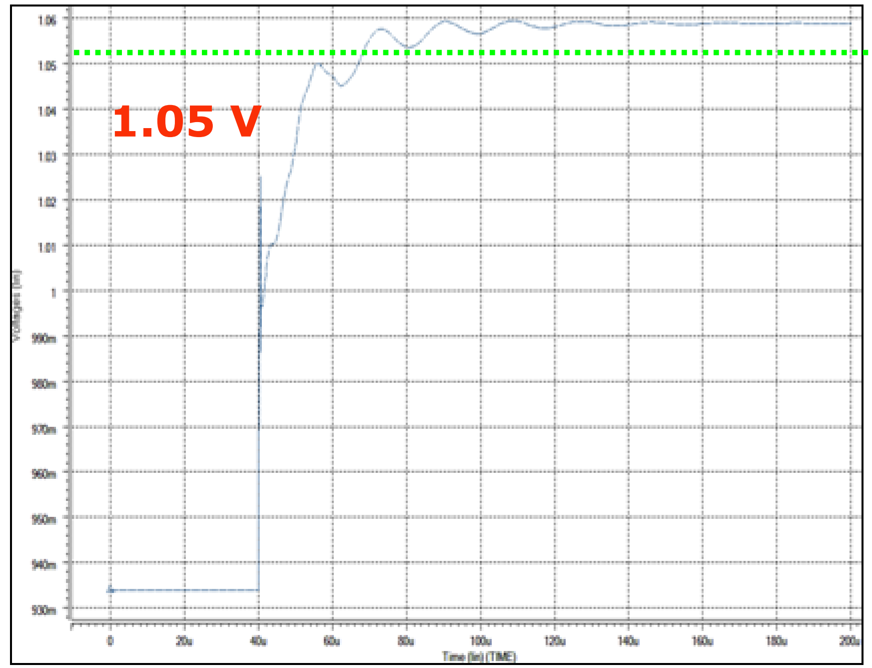
- Introduction
- Simplified SPICE Model
- Case Study and Its Application
- ✓ Validation
- Summary & Next Steps

XYZ CRB
Simulation Result vs. VRTT Test Result

Loading frequency = 305 Hz

Slew=163 A/uS





1st spike reading:

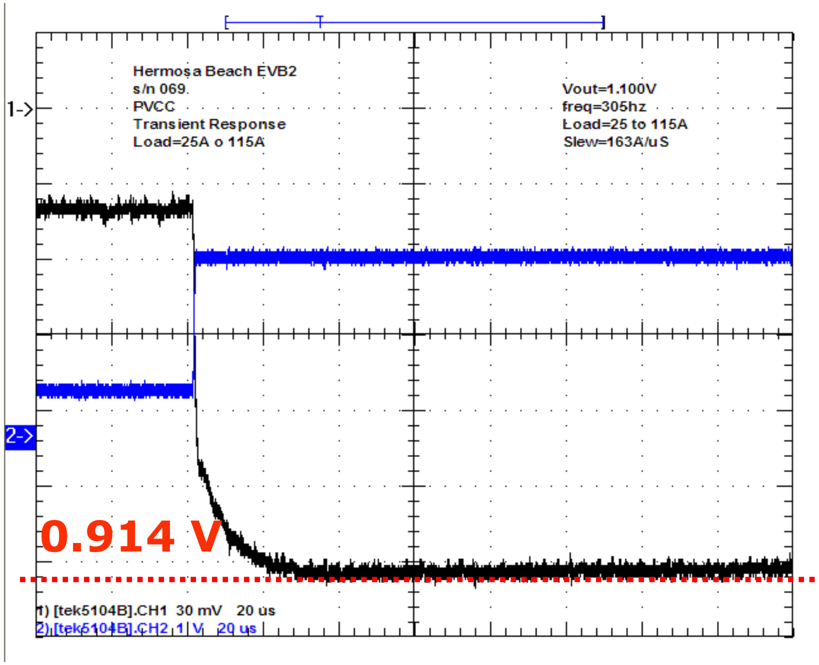
1.058 V vs. 1.05 V @ 115 A to 25 A **8 mV** difference only → **99.24% Accuracy**

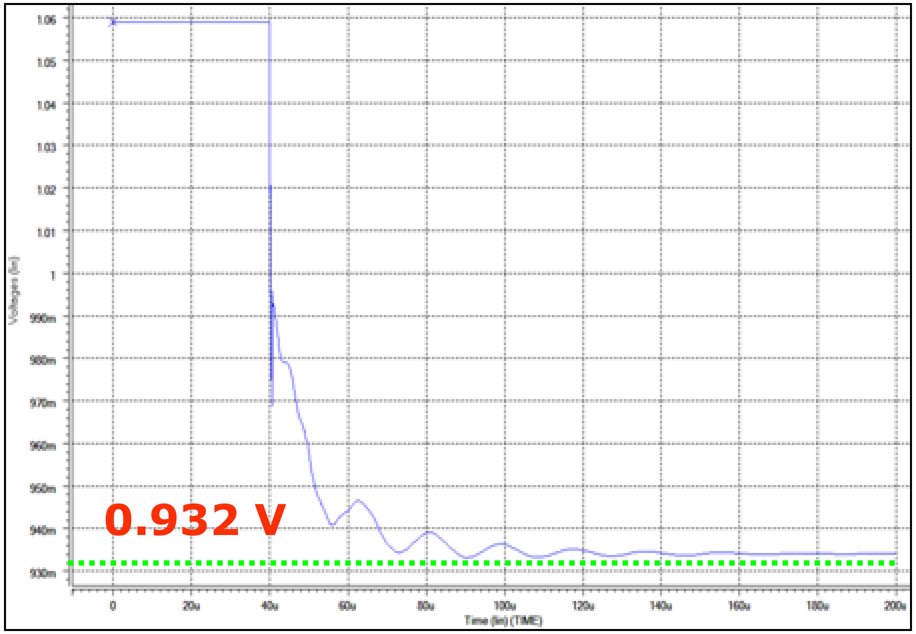
- Including more sophisticated VR model with FETs may be able to reduce Waveform Δ.
- Adding MB parasitic C & L should be helpful in reduction of waveform Δ as well.

XYZ CRB
Simulation Result vs. VRTT Test Result

Loading frequency = 305 Hz

Slew=163 A/uS





1st spike reading:

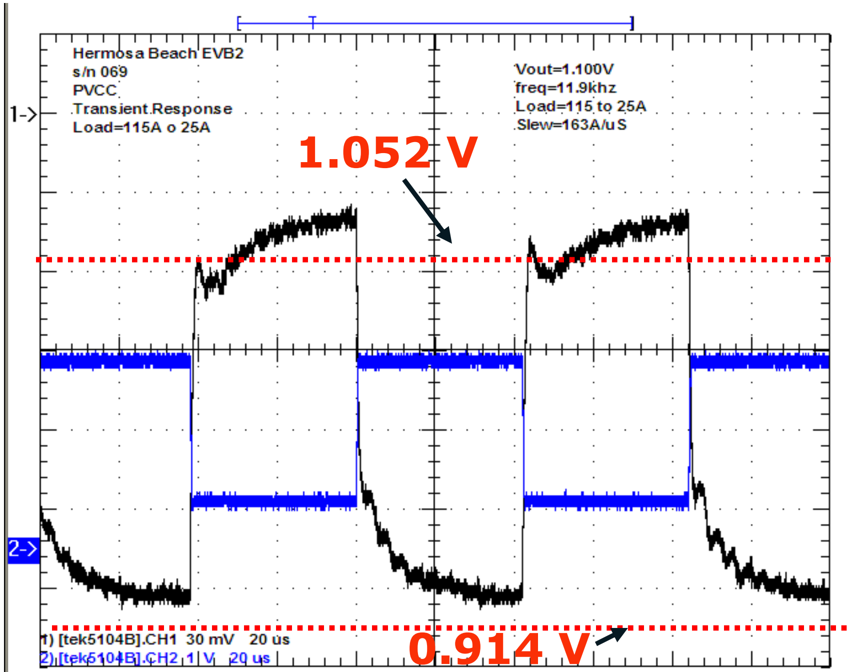
0.914 V vs. 0.932 V @ 25 A to 115 A **18 mV** difference only → **98.07% Accuracy**

- Including more sophisticated VR model with FETs may be able to reduce Waveform Δ.
- Adding MB parasitic C & L should be helpful in reduction of waveform Δ as well.

XYZ CRB
Simulation Result vs. VRTT Test Result

Loading frequency = 12K

Slew=163A/uS



1st spike reading:

1.052 V vs. 1.054 V @ **115** A to 25 A **2 mV** difference only → **99.8% Accuracy**

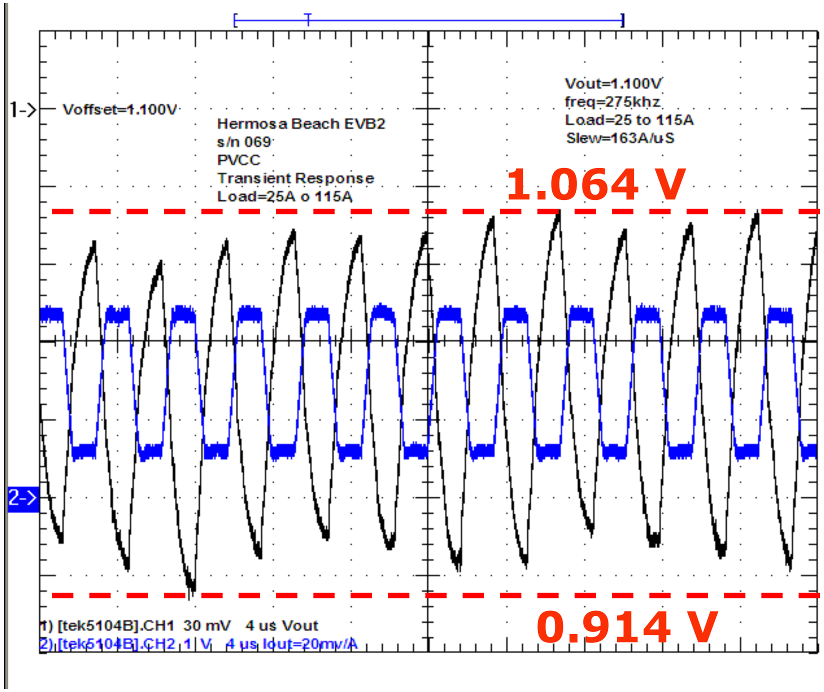
0.914 V vs. 0.934 V @ 25 A to 115 A **20 mV** difference only → **97.85% Accuracy**

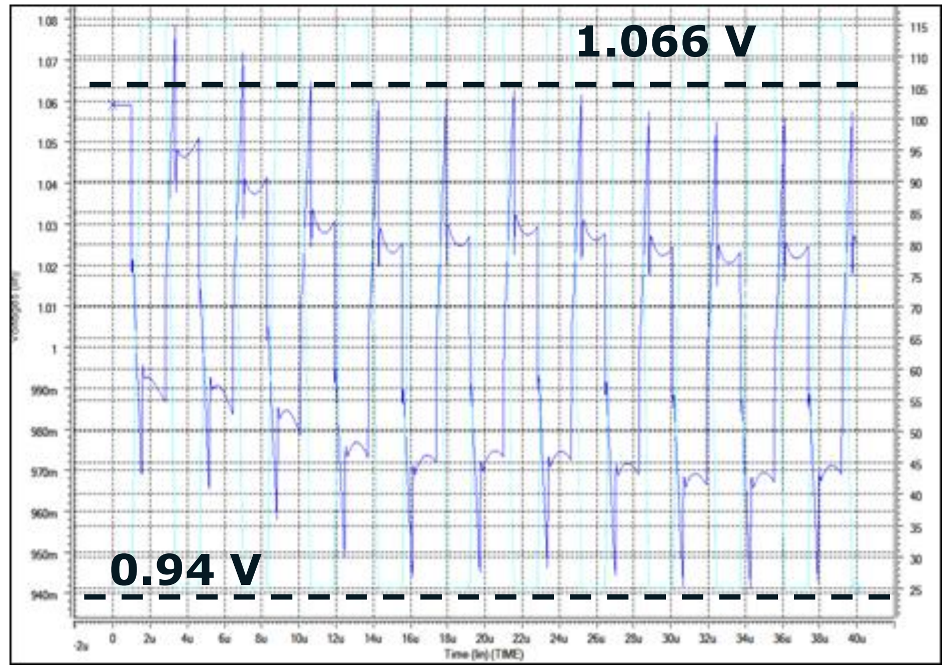
- Including more sophisticated VR model with FETs may be able to reduce Waveform ∆.
- Adding MB parasitic C & L should be helpful in reduction of waveform ∆ as well.

XYZ CRB
Simulation Result vs. VRTT Test Result

Loading frequency = 275K

Slew=163 A/uS





1st spike reading:

1.064 V vs. 1.066 V @ 115 A to 25 A **2 mV** difference only → **99.8% Accuracy**

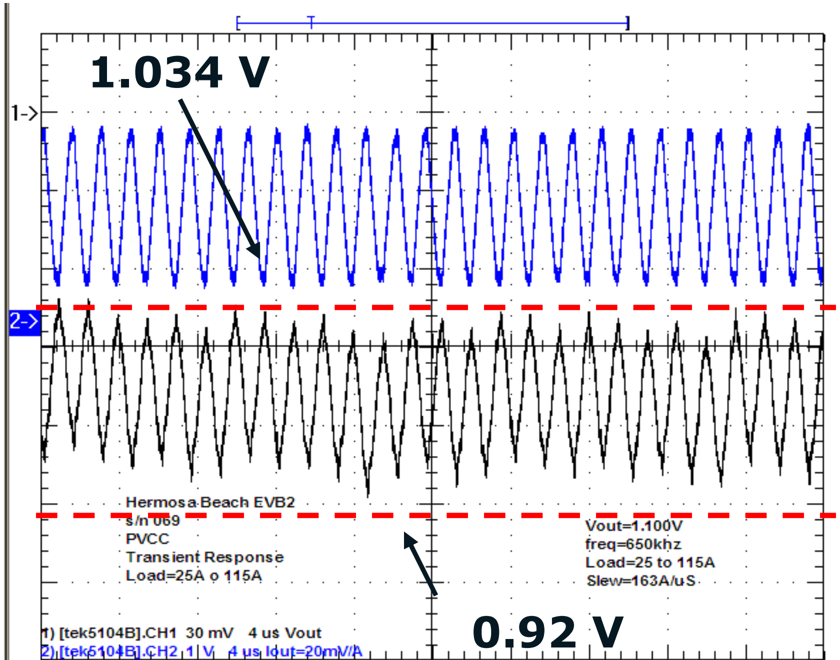
0.914 V vs. 0.94 V @ 25 A to 115 A **26 mV** difference only → **97.63% Accuracy**

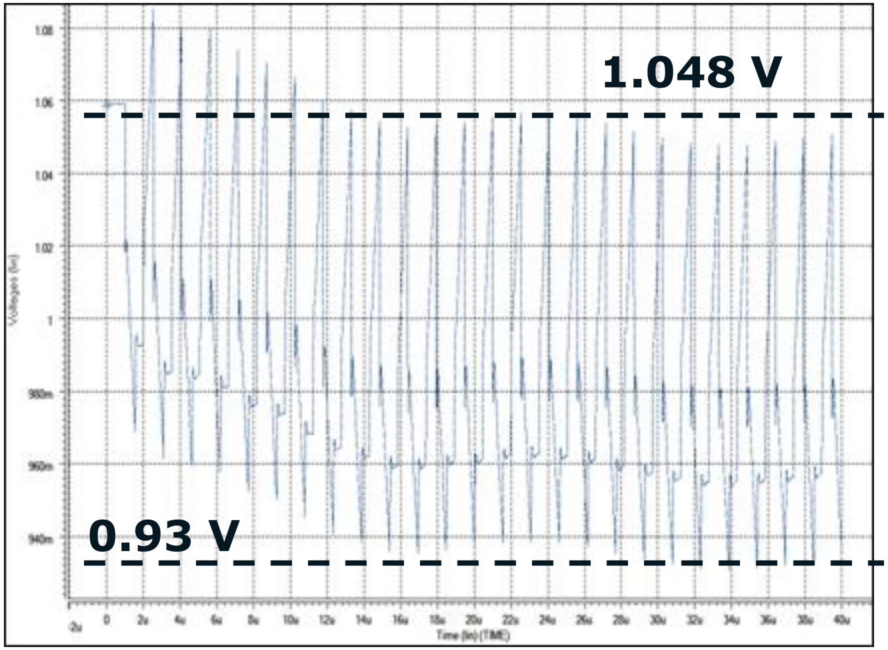
- Including more sophisticated VR model with FETs may be able to reduce Waveform Δ.
- Adding MB parasitic C & L should be helpful in reduction of waveform Δ as well.

XYZ CRB
Simulation Result vs. VRTT Test Result

Loading frequency = 650K

Slew=163 A/uS





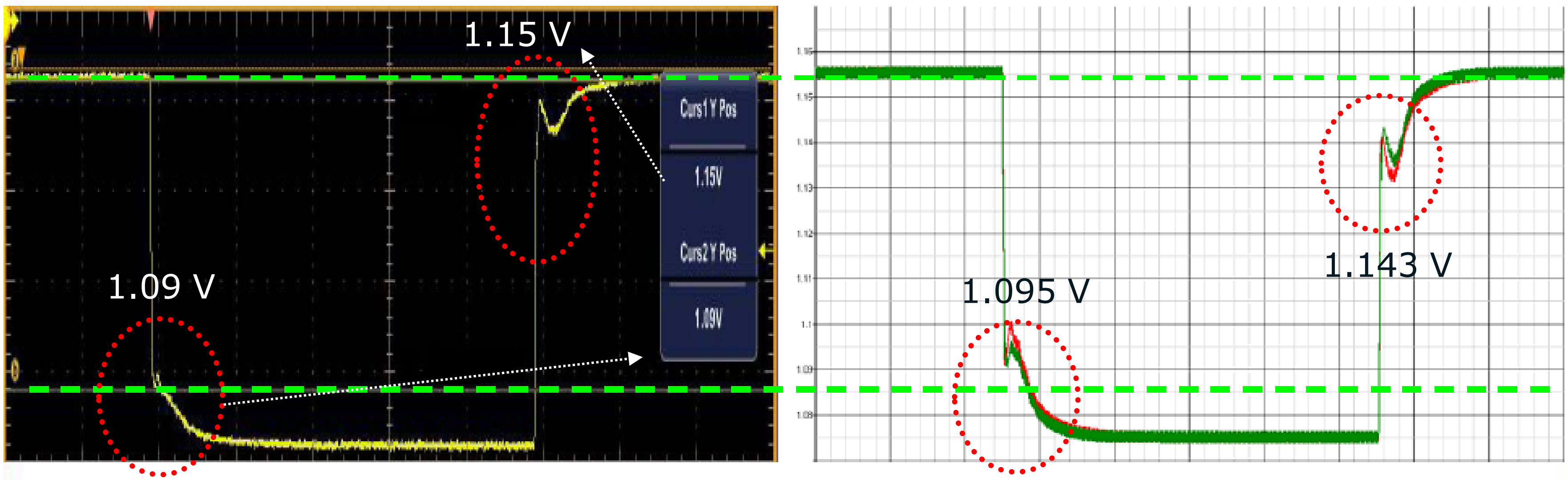
1st spike reading:

1.034 V vs. 1.048 V @ 115 A to 25 A **14 mV** difference only → **98.66% Accuracy**

0.92 V vs. 0.93 V @ 25 A to 115 A **10 mV** difference only → **98.9% Accuracy**

- Including more sophisticated VR model with FETs may be able to reduce Waveform Δ.
- Adding MB parasitic C & L should be helpful in reduction of waveform Δ as well.

Simulation Result vs. Real VRTT Test Result



— MB model is a Resistance network
— MB model is a SPICE lump circuit

1st spike reading:

1.15 V vs. 1.143 V @ 165 A to 59 A **7 mV** difference only

1.09 V vs. 1.095 V @ 59 A to 165 A **5 mV** difference only

Simulation Result Accuracy higher then 99%
*** (This case used a very sophisticated VR model from VR Vender.)**

Agenda

- Introduction
- Simplified SPICE Model
- Case Study & Its Application
- Methodology Validation

✓ Summary and Next Steps

Summary and Next Steps

Simplified SPICE model has been validated by companies

Using the collaterals, companies can

- optimize their own designs & make their own decisions before Gerber Out to achieve the best cost/performance trade-off in
  - Determine # of MB layers & stack-up
  - Choose MB cap types, numbers & locations
- reduce risk of common ground noise coupling among Vcc, Vsa, Vtt, and Vddq
- validate their own designs after Gerber Out

Next Steps

- Obtain more sophisticated VR model from venders
- Include thermal impact to more accurately predict Maximum Current can be carried.