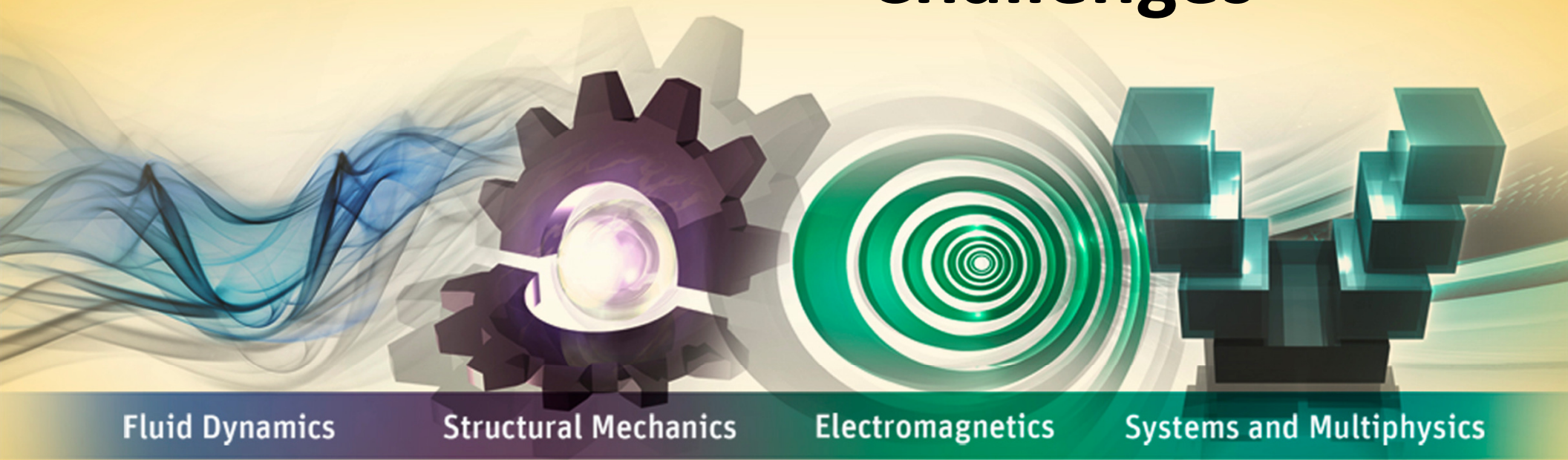


Electronic Interconnect Challenges



Fluid Dynamics

Structural Mechanics

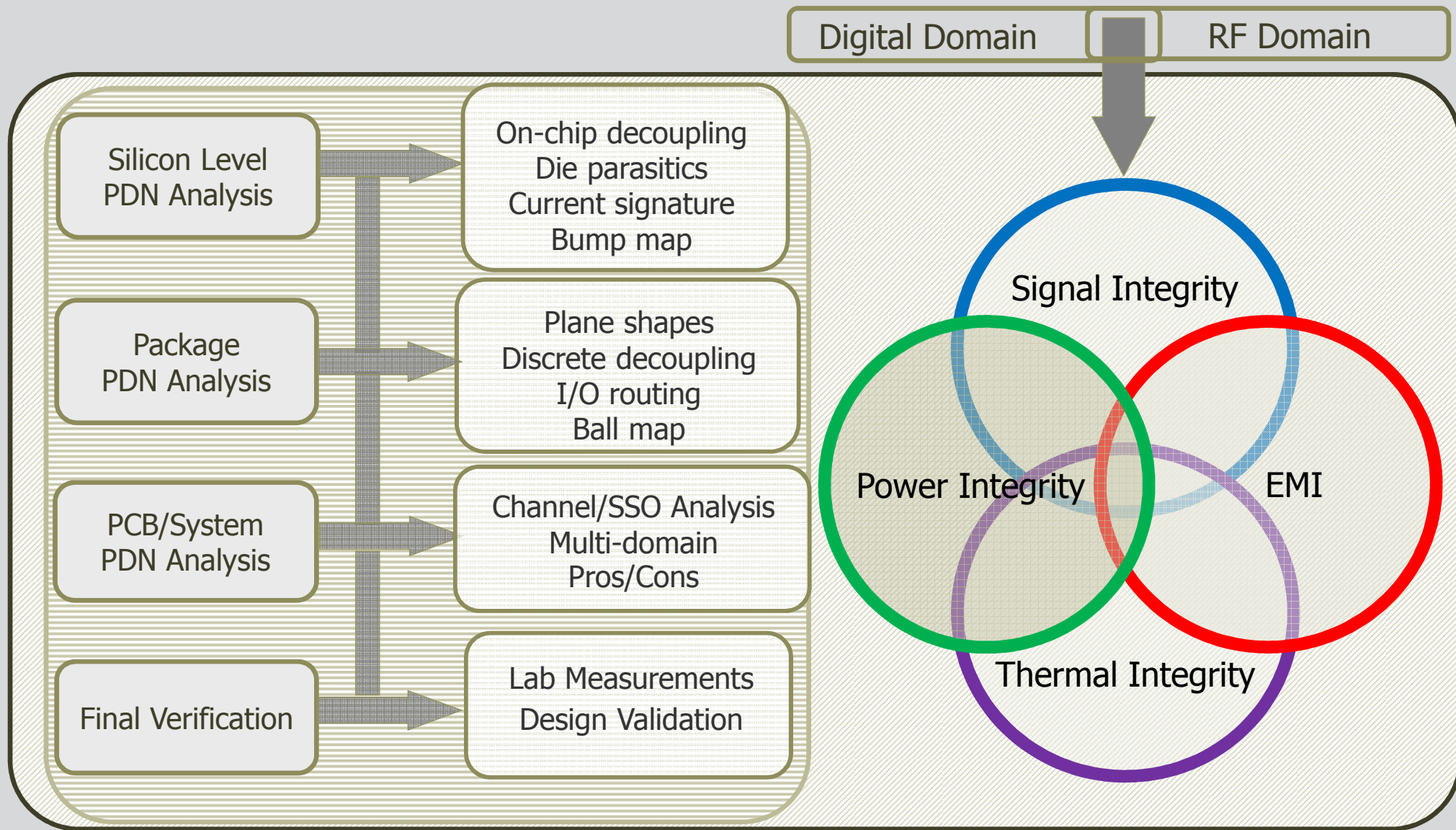
Electromagnetics

Systems and Multiphysics

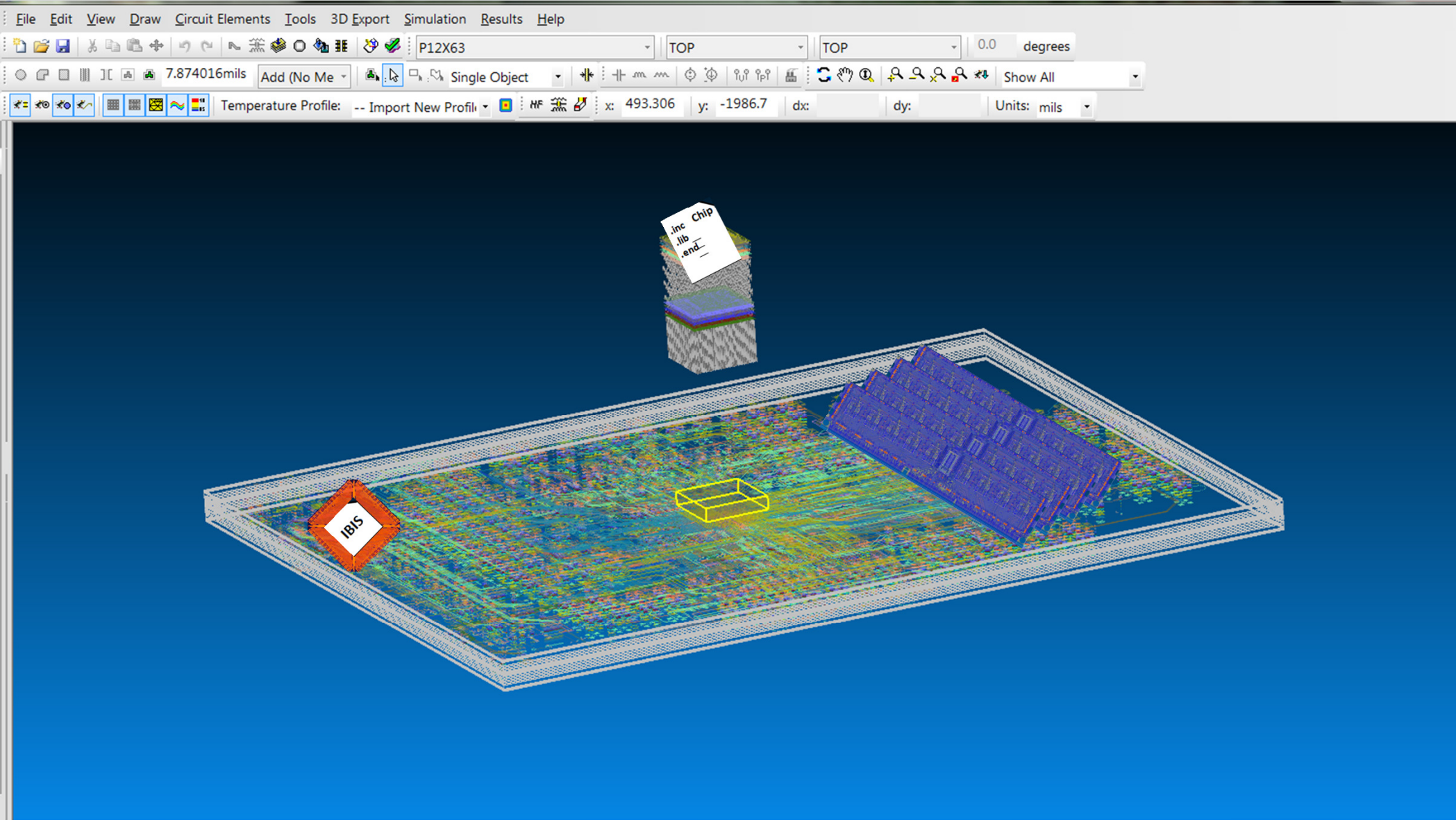
Asian IBIS Summit
Hsinchu, Taiwan
November 13, 2012

Steven G. Pytel, PhD.
SI Product Manager

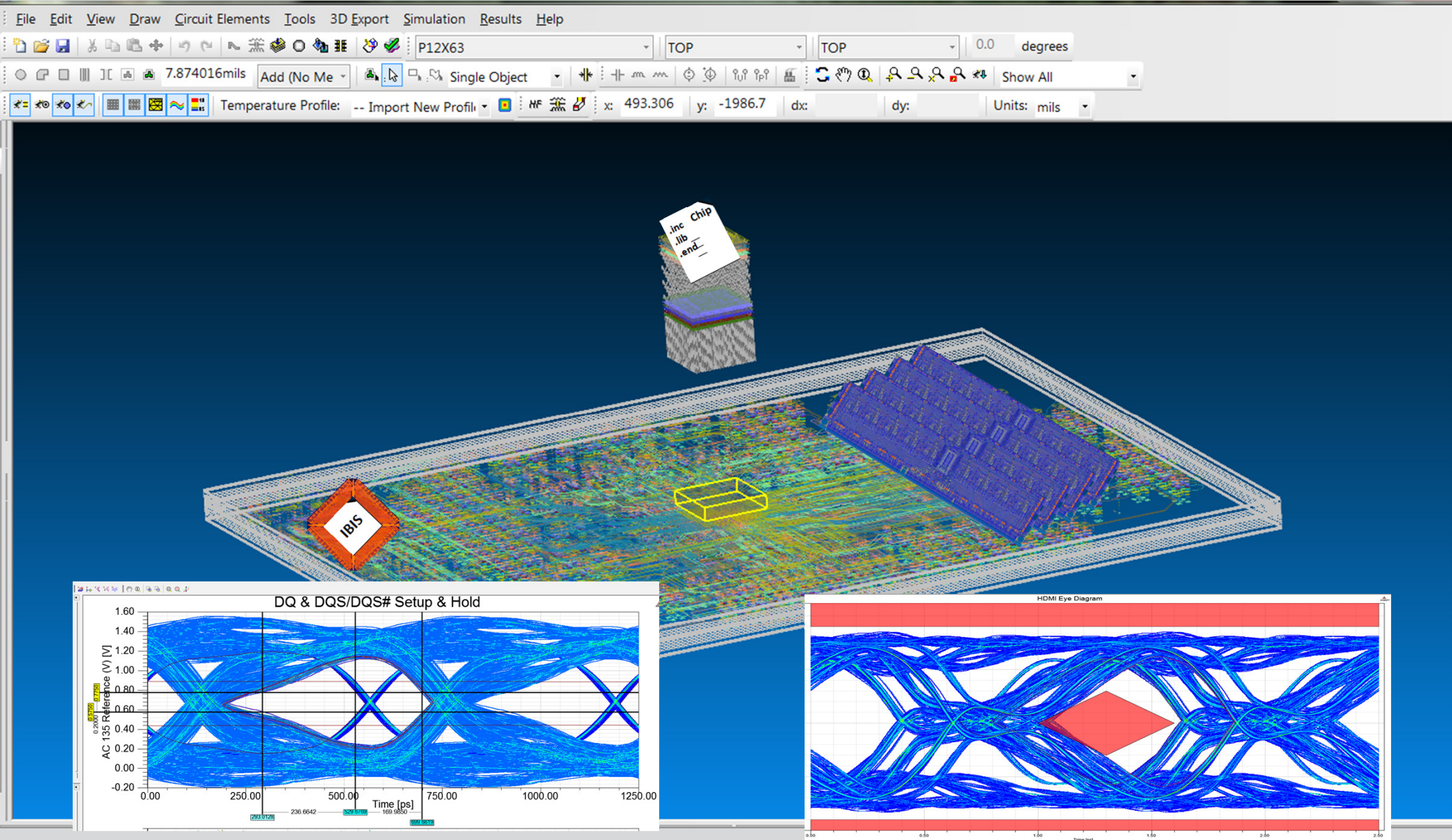
Chip Aware System Design



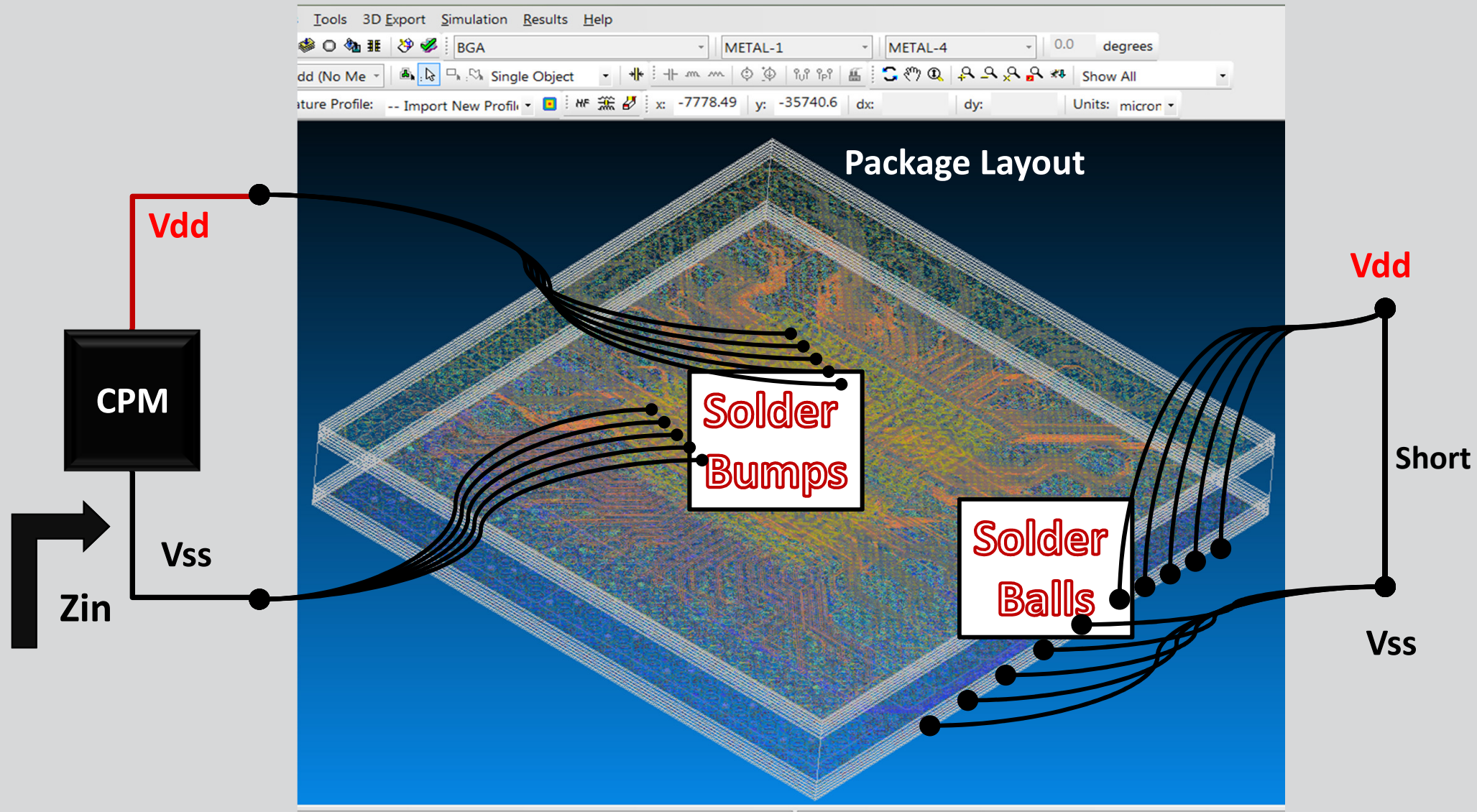
Virtual Platform for System Design



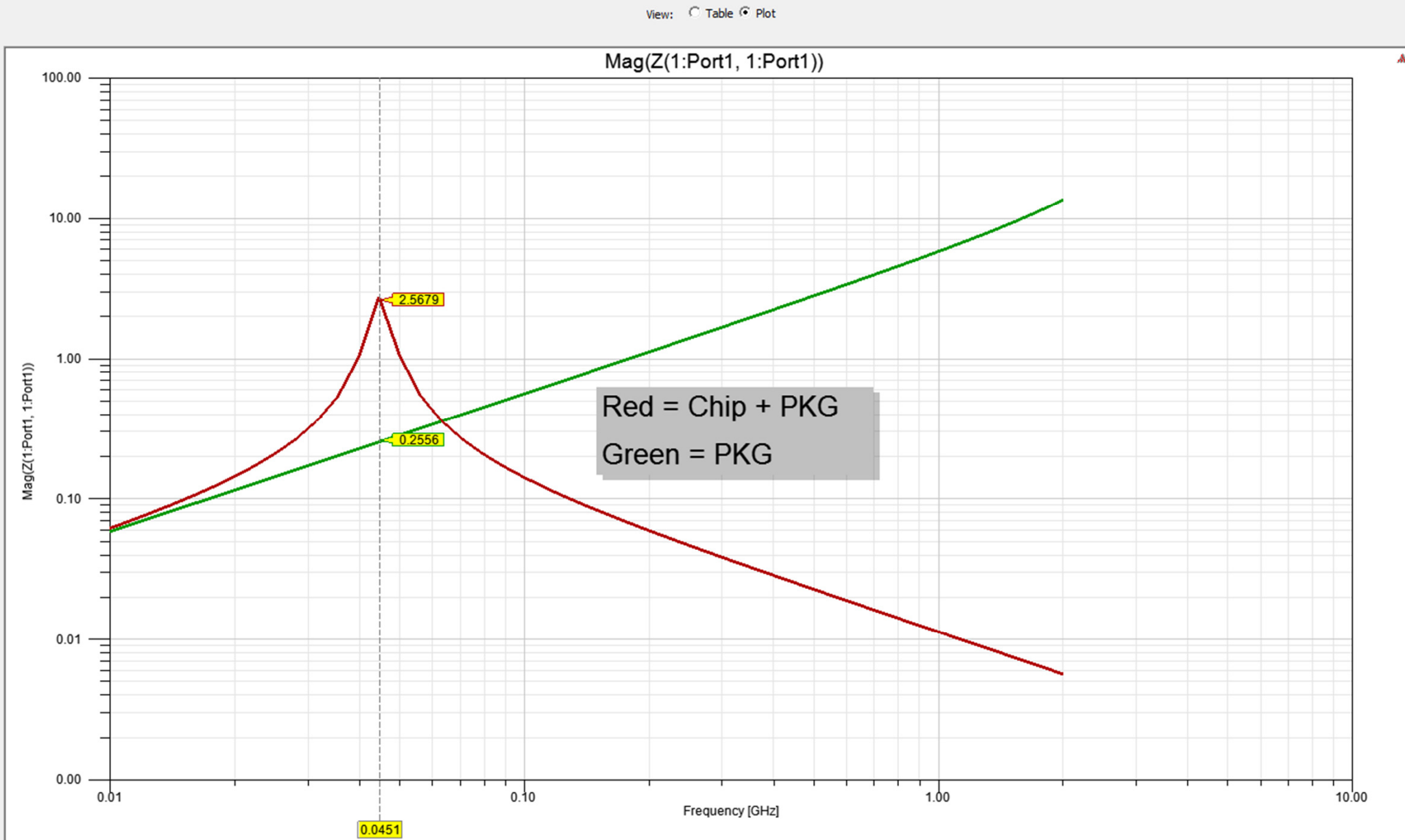
Virtual Platform for System Design



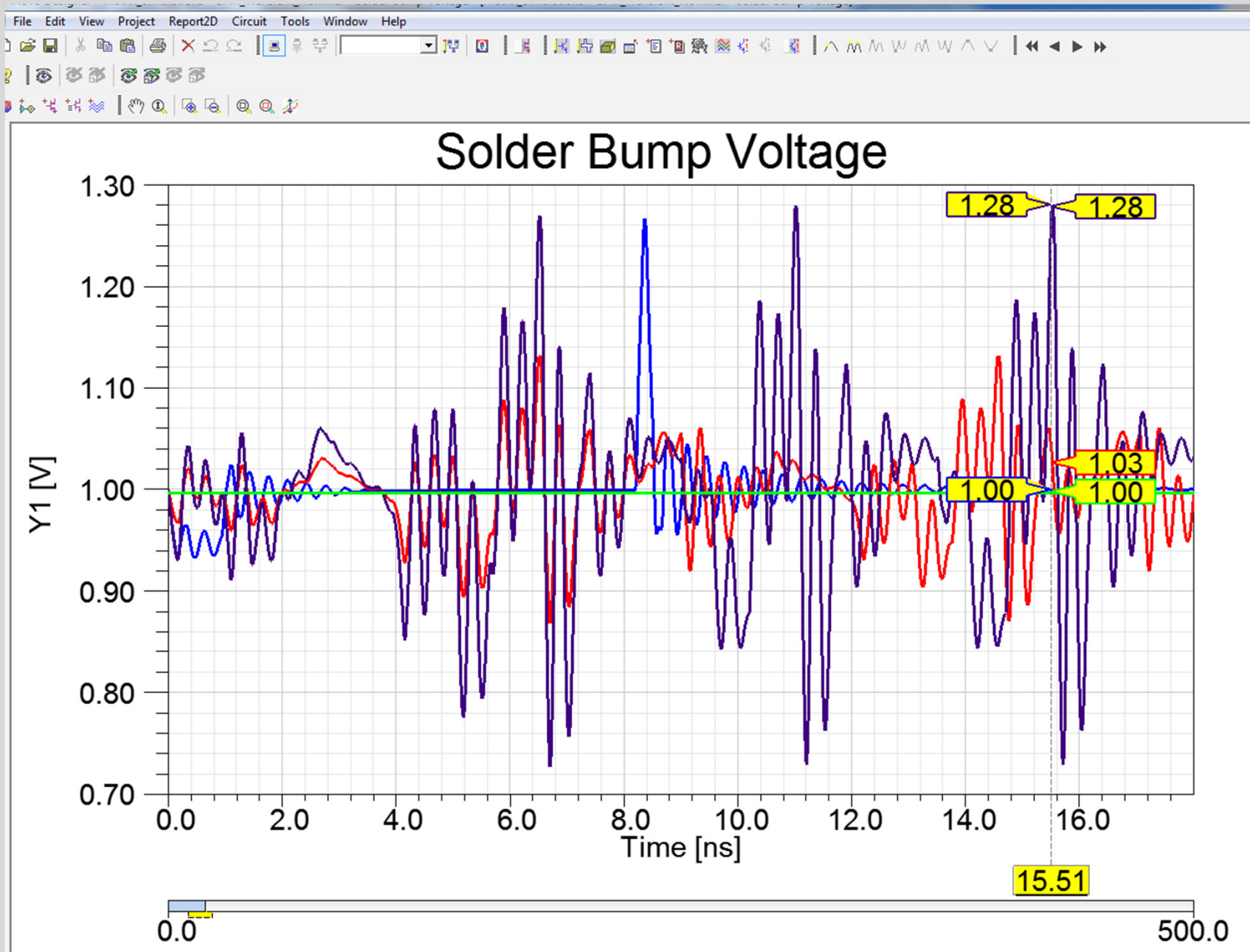
Extraction of Input Impedance



Impedance Results with & without Chip



Die Solder Bump Voltage



Digital Domain

RF Domain

Silicon Level
PDN Analysis

On-chip decoupling
Die parasitics
Current signature
Bump map

Package
PDN Analysis

Plane shapes
Discrete decoupling
I/O routing
Ball map

PCB/System
PDN Analysis

Channel/SSO Analysis
Multi-domain
Pros/Cons

Final Verification

Lab Measurements
Design Validation

- **Chip RLC parasitics change system performance**
- **Chip current signatures change system performance**
- **Interconnect design must include Chip-Chip effect**

