

IBIS Interconnect BIRD Update

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Overview

- IBIS Interconnect Task Group
- Models Represent Package and On-Die Interconnect
- On Die, Package, Supply and Signal Interconnect can be Combined or Kept Separate
- IBIS Interconnect Model Terminals
- Examples

IBIS Interconnect Task Group

- Meets Wednesdays 8AM PDT
- http://www.ibis.org/interconnect_wip/
- Major Contributors
 - Altera David Banas
 - Cadence Design Systems Bradley Brim
 - Intel Corp Michael Mirmak (Chair)
 - Keysight Technologies Radek Biernacki
 - Mentor Graphics Arpad Muranyi
 - Micron Technology Justin Butterfield, Randy Wolff
 - Signal Integrity Software Walter Katz, Mike LaBonte
 - Synopsys Rita Horner
 - Teraspeed Labs Bob Ross

Models Represent Package and On-Die Interconnect

- Currently IBIS supports lumped coupled RLC models or lossless uncoupled distributed models.
- New modeling will support broadband, coupled, signal interconnect and power distribution models.
- Languages Supported
 - IBIS-ISS
 - IBIS Interconnect SPICE Subcircuit (IBIS-ISS) Specification, Version 1.0, October 7th 2011
http://www.ibis.org/ibis-iss_ver1.0/ibis-iss_ver1_0.pdf
 - Touchstone[®]
 - http://www.ibis.org/touchstone_ver2.0/

On Die, Package, Supply and Signal Interconnect can be Combined or Kept Separate

- Supports separate on-die and package interconnect models and combined on-die and package interconnect models
- Independent Supply and Signal Interconnect Models
- Coupled Supply and Signal Interconnect Models
- Singled Ended and Differential Interconnect Models

Similar Approach for Both IBIS and EBD

- IBIS (.ibs) Interconnect Model Terminals
 - Pins ([Pins])
 - Die Pads
 - Buffers
- EBD (.ebd) Interconnect Model Terminals
 - A similar approach will be used to update EBD (Electrical Board Description) or EMD (Electrical Module Description) to support broadband, coupled interconnect models

IBIS Interconnect Model Terminals

- Pins
 - Pin_name (aka Pin Number)
 - Signal_name (assumes signal_name pins shorted)
 - Bus_label (allows sub-groups of rail signal_name pins)
- Pads (Die/Package Interface)
 - Pin_name (aka Pin Number) for I/O connections
 - Pad_name for rail connections
 - Signal_name (assumes signal_name pads shorted)
 - Bus_label (allows sub-groups of rail signal_name pads)
- Buffers
 - Signal (I/O)
 - Rails
 - Pin_name and (puref/pdref/pcref/gcref)
 - Signal_name (assumes signal_name terminals shorted)
 - Bus_label (allows sub-groups of rail buffer terminals)

Interconnect Model Terminals

- <Terminal Number> <Terminal Type> <Qualifier>
 - X: I/O pin_name
 - Y: Supply pin_name, signal_name or bus_label
 - Z: Supply pad_name

Terminal_Type	pin_name	signal_name	bus_label	pad_name
Buffer_I/O	X			
Puref	X			
Pdref	X			
Pceref	X			
Gceref	X			
Extref	X			
Buffer_rail		Y	Y	
Pad_I/O	X			
Pad_rail		Y	Y	Z
Pin_I/O	X			
Pin_rail	Y	Y	Y	

Interconnect Model Examples

```
[Interconnect Model]    DQ1    | IBIS-ISS Model
File_IBIS-ISS          DQ.iss    DQ
Param Length Value    0.1
Number_of_Terminals = 2
1 Pin_I/O              pin_name    A1
2 Buffer_I/O           pin_name    A1
[End Interconnect Model]
```

```
[Interconnect Model]    A1    | Touchstone File Shortcut
File_TS                A1.s2p
Number_of_Terminals = 3
1 Pin_I/O              pin_name    A1
2 Buffer_I/O           pin_name    A1
3 Pin_rail             signal_name VSS
[End Interconnect Model]
```

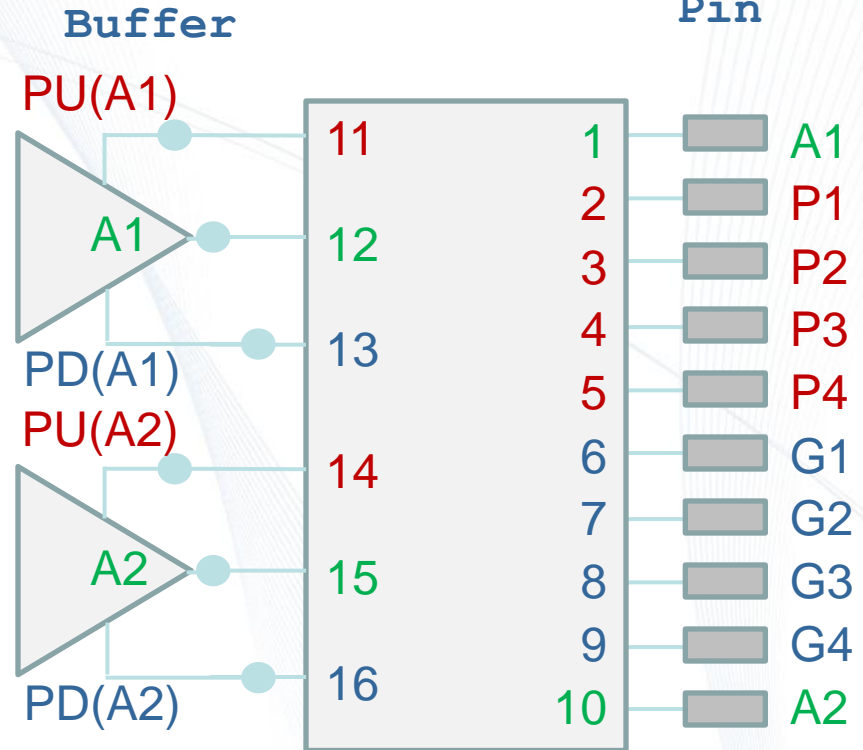
Full Package, All Pins to All Buffers

[Pin]	signal_name	model_name
A1	DQ1	DQ
A2	DQ2	DQ
P1	VDD	POWER
P2	VDD	POWER
P3	VDD	POWER
P4	VDD	POWER
G1	VSS	GND
G2	VSS	GND
G3	VSS	GND
G4	VSS	GND

[Begin Interconnect Model]

```

...
1 Pin_I/O pin_name A1
2 Pin_rail pin_name P1
3 Pin_rail pin_name P2
4 Pin_rail pin_name P3
5 Pin_rail pin_name P4
6 Pin_rail pin_name G1
7 Pin_rail pin_name G2
8 Pin_rail pin_name G3
9 Pin_rail pin_name G4
10 Pin_I/O pin_name A2
11 Puref pin_name A1
12 Buffer_I/O pin_name A1
13 Pdref pin_name A1
14 Puref pin_name A2
15 Buffer_I/O pin_name A2
16 Pdref pin_name A2
[End Interconnect Model]
    
```



```
.subckt AllPinsAllBuffers 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
```

Full Package, All VDD and VSS Pins Shorted All Buffer Rail Connections Shorted on Die

```
[Pin]      signal_name  model_name
A1         DQ1         DQ
A2         DQ2         DQ
P1         VDD         POWER
P2         VDD         POWER
P3         VDD         POWER
P4         VDD         POWER
G1         VSS         GND
G2         VSS         GND
G3         VSS         GND
G4         VSS         GND
```

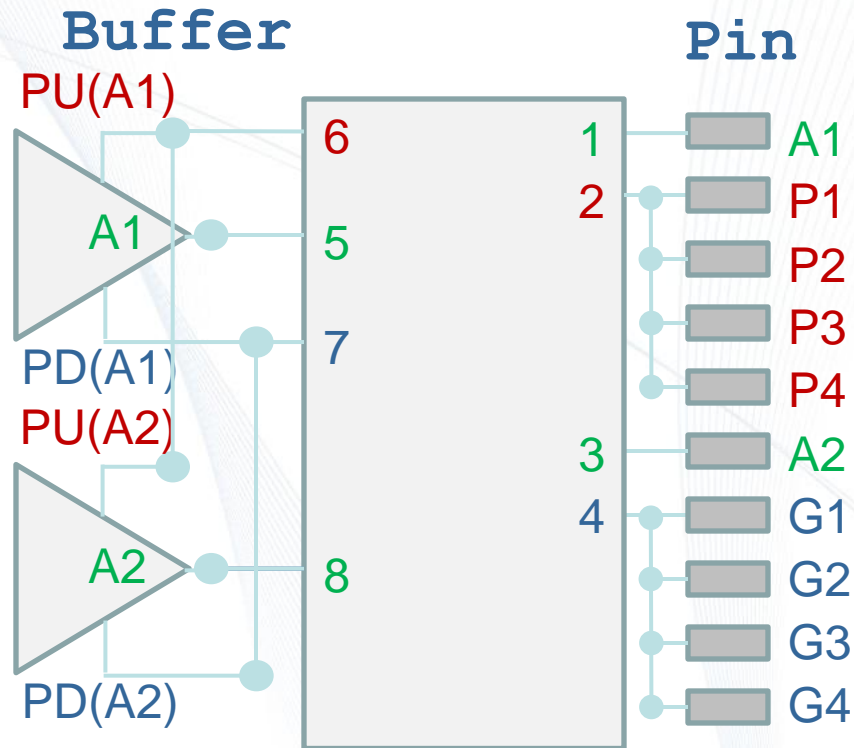
```
[Pin Mapping] pulldown_ref pullup_ref
Bus_label_signal_name
A1             VSS         VDD
A2             VSS         VDD
```

```
[Begin Interconnect Model]
```

```
...
1  Pin_I/O      pin_name      A1
2  Pin_rail     signal_name   VDD
3  Pin_I/O      pin_name      A2
4  Pin_rail     signal_name   VSS
5  Buffer_I/O   pin_name      A1
6  Buffer_rail  signal_name   VDD
7  Buffer_rail  signal_name   VSS
8  Buffer_I/O   pin_name      A2
```

```
[End Interconnect Model]
```

```
.subckt AllPinsRailsShorted 1 2 3 4 5 6 7 8
```



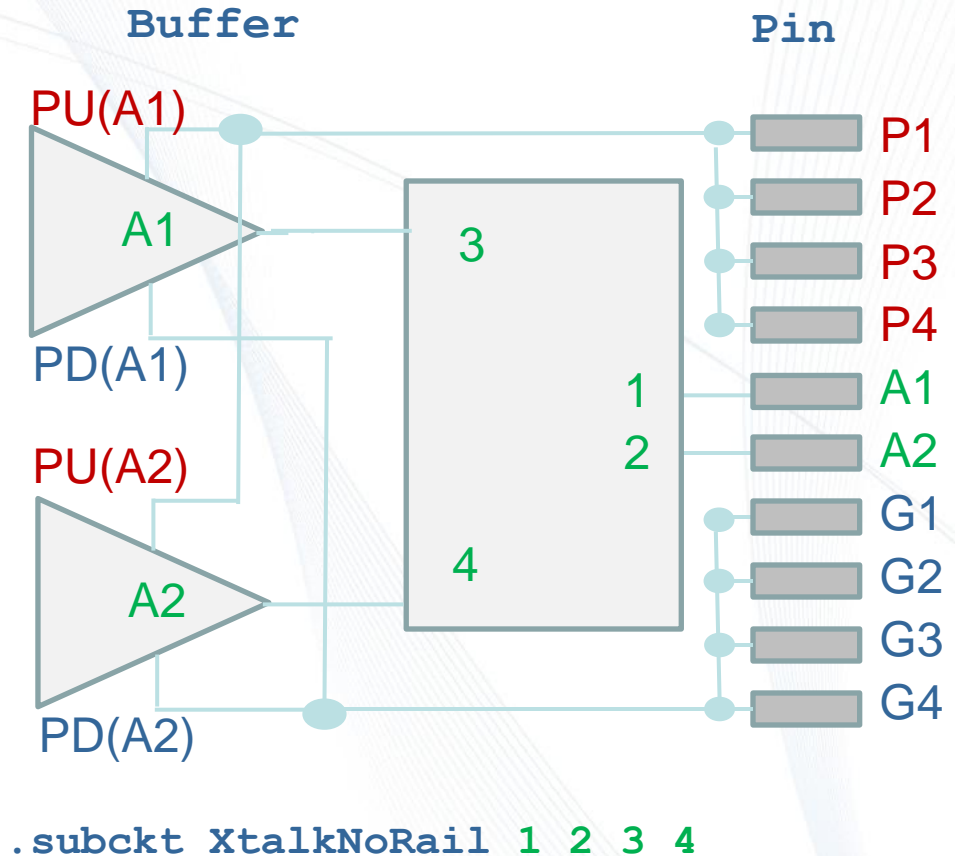
Crosstalk Model, Signal I/O Only

```
[Pin]      signal_name  model_name
A1         DQ1         DQ
A2         DQ2         DQ
P1         VDD         POWER
P2         VDD         POWER
P3         VDD         POWER
P4         VDD         POWER
G1         VSS         GND
G2         VSS         GND
G3         VSS         GND
G4         VSS         GND
```

```
[Pin Mapping] pulldown_ref pullup_ref
Bus_label_signal_name
A1             VSS         VDD
A2             VSS         VDD
```

```
[Begin Interconnect Model]
```

```
...
1  Pin_I/O      pin_name  A1
2  Pin_I/O      pin_name  A2
3  Buffer_I/O   pin_name  A1
4  Buffer_I/O   pin_name  A2
[End Interconnect Model]
```

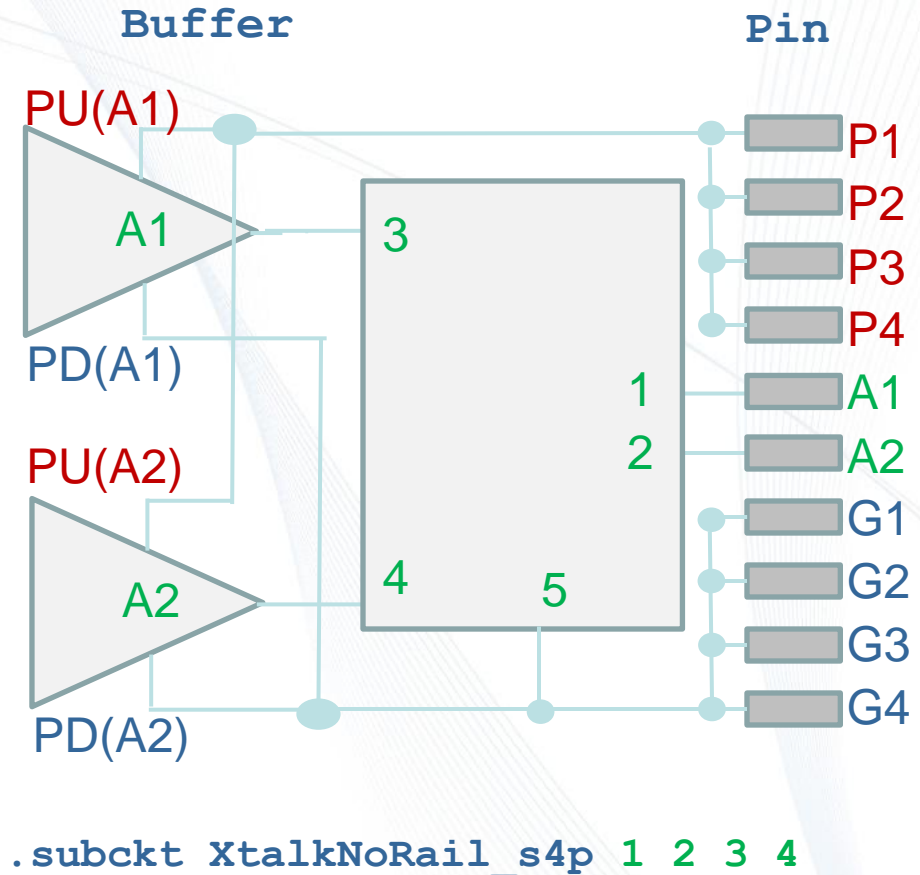


Crosstalk Model, Signal I/O Only, Touchstone Model

```
[Pin]      signal_name  model_name
A1         DQ1         DQ
A2         DQ2         DQ
P1         VDD         POWER
P2         VDD         POWER
P3         VDD         POWER
P4         VDD         POWER
G1         VSS         GND
G2         VSS         GND
G3         VSS         GND
G4         VSS         GND
```

```
[Pin Mapping] pulldown_ref pullup_ref
Bus_label_signal_name
A1             VSS         VDD
A2             VSS         VDD
```

```
[Begin Interconnect Model]
File TS xyz.s4p
1  Pin_I/O      pin_name    A1
2  Pin_I/O      pin_name    A2
3  Buffer_I/O   pin_name    A1
4  Buffer_I/O   pin_name    A2
5  Pin_rail     signal_name VSS
[End Interconnect Model]
```



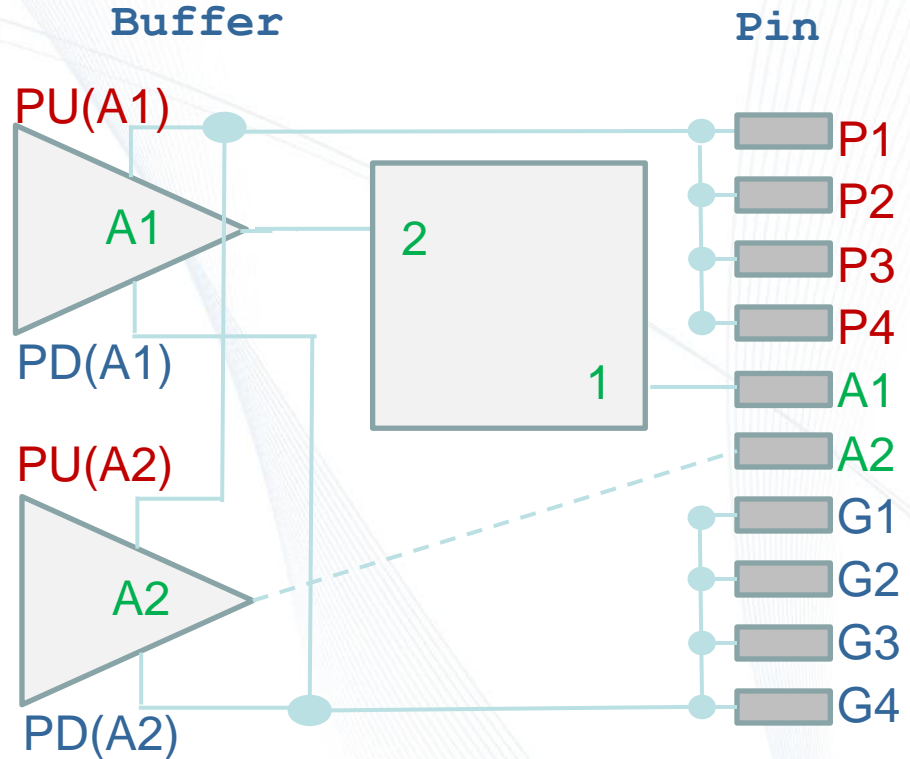
DQ1 Pin to Buffer

```
[Pin]      signal_name  model_name
A1         DQ1         DQ
A2         DQ2         DQ
P1         VDD         POWER
P2         VDD         POWER
P3         VDD         POWER
P4         VDD         POWER
G1         VSS         GND
G2         VSS         GND
G3         VSS         GND
G4         VSS         GND
```

```
[Pin Mapping] pulldown_ref pullup_ref
Bus_label_signal_name
A1             VSS           VDD
A2             VSS           VDD
```

```
[Begin Interconnect Model]
```

```
...
1  Pin I/O      pin_name  A1
2  Buffer I/O   pin_name  A1
[End Interconnect Model]
```



```
.subckt DQ1Pin2Buffer 1 2
```

DQ1 Pin to Pad, DQ1 Pad to Buffer

```
[Pin]      signal_name  model_name
A1         DQ1         DQ
A2         DQ2         DQ
P1         VDD         POWER
P2         VDD         POWER
P3         VDD         POWER
P4         VDD         POWER
G1         VSS         GND
G2         VSS         GND
G3         VSS         GND
G4         VSS         GND
```

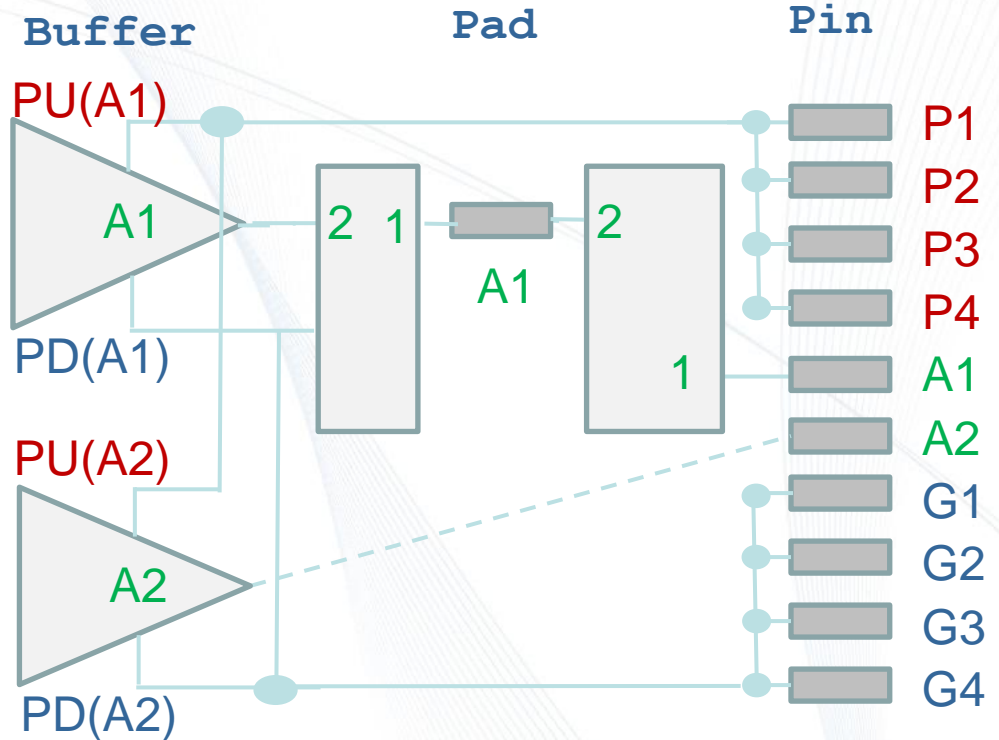
```
[Pin Mapping] pulldown_ref pullup_ref
Bus_label_signal_name
A1         VSS         VDD
A2         VSS         VDD
```

[Begin Interconnect Model]

```
...
1  Pin I/O      pin_name  A1
2  Pad I/O     pin_name  A1
[End Interconnect Model]
```

[Begin Interconnect Model]

```
...
1  Pad I/O      pin_name  A1
2  Buffer I/O   pin_name  A1
[End Interconnect Model]
```



```
.subckt DQ1Pin2Pad 1 2
.subckt DQ1Pad2Buffer 1 2
XPinPad PinA1 PadA1 DQ1Pin2Pad
XPadBuf PadA1 BufA1 DQ1Pad2Buffer
```

VDD Pad by signal_name

[Pin]	signal_name	model_name
A1	DQ1	DQ
A2	DQ2	DQ
P1	VDD	POWER
P2	VDD	POWER
P3	VDD	POWER
P4	VDD	POWER
G1	VSS	GND
G2	VSS	GND
G3	VSS	GND
G4	VSS	GND

[Pin Mapping]	pulldown_ref	pullup_ref
Bus_label_signal_name		
A1	VSS	VDD
A2	VSS	VDD

[Die Supply Pads]	signal_name	bus_label
VDD1	VDD	VDDa
VDD2	VDD	VDDa
VDD3	VDD	VDDb

[End Die Supply Pads]

[Begin Interconnect Model]

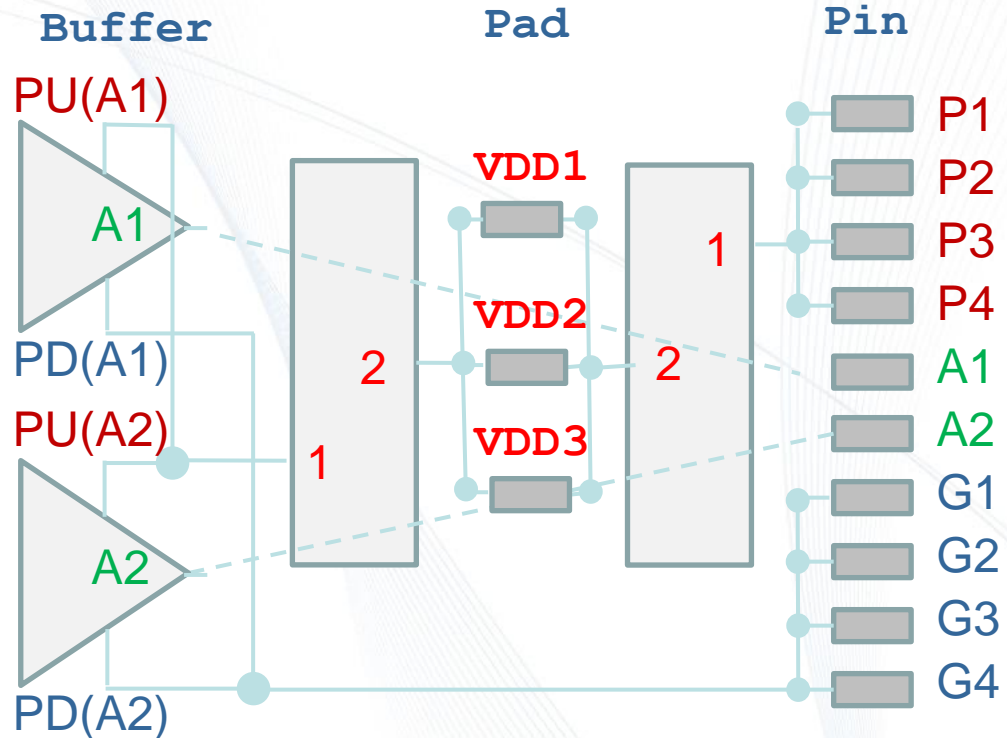
...			
1	Pin_rail	signal_name	VDD
2	Pad_rail	signal_name	VDD

[End Interconnect Model]

[Begin Interconnect Model]

...			
1	Buffer_rail	signal_name	VDD
2	Pad_rail	signal_name	VDD

[End Interconnect Model]



```
.subckt VDDPin2Pad_sn 1 2
```

```
.subckt VDDBuf2Pad_sn 1 2
```

```
XPinPad VDDPin VDDPad VDDPin2Pad_sn
```

```
XBufPad VDDPad VDDBuf VDDBuf2Pad_sn
```

VDD Pad by pad_name

```

[Pin]      signal_name  model_name
A1         DQ1          DQ
A2         DQ2          DQ
P1         VDD          POWER
P2         VDD          POWER
P3         VDD          POWER
P4         VDD          POWER
G1         VSS          GND
G2         VSS          GND
G3         VSS          GND
G4         VSS          GND

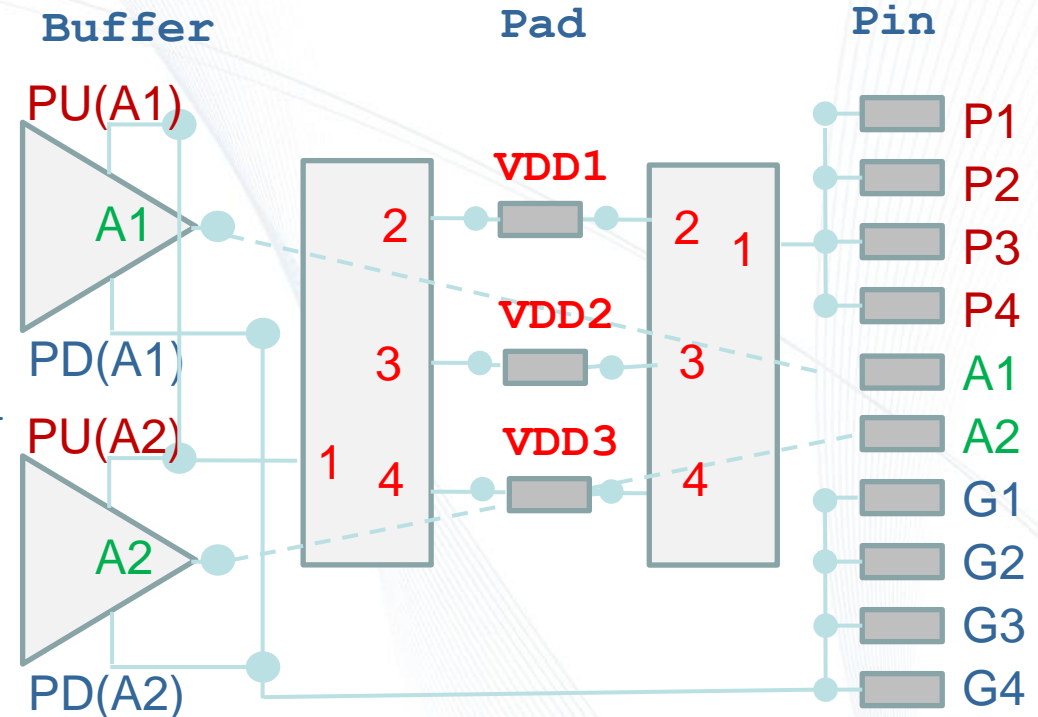
[Pin Mapping] pulldown_ref pullup_ref
Bus_label_signal name
A1            VSS          VDD
A2            VSS          VDD

[Die Supply Pads] signal_name bus_label
VDD1           VDD          VDDa
VDD2           VDD          VDDa
VDD3           VDD          VDDb
[End Die Supply Pads]

[Begin Interconnect Model]
...
1 Pin_rail      signal_name  VDD
2 Pad_rail      pad_name     VDD1
3 Pad_rail      pad_name     VDD2
4 Pad_rail      pad_name     VDD3
[End Interconnect Model]

[Begin Interconnect Model]
...
1 Buffer_rail   signal_name  VDD
2 Pad_rail      pad_name     VDD1
3 Pad_rail      pad_name     VDD2
4 Pad_rail      pad_name     VDD3
[End Interconnect Model]

```



```

.subckt VDDPin2Pad 1 2 3 4
.subckt VDDBuf2Pad 1 2 3 4

XPinPad VDDPin VDD1 VDD2 VDD3 VDDPin2Pad
XBufPad VDDBuf VDD1 VDD2 VDD3 VDDBuf2Pad

```

VDD Pad by bus_label

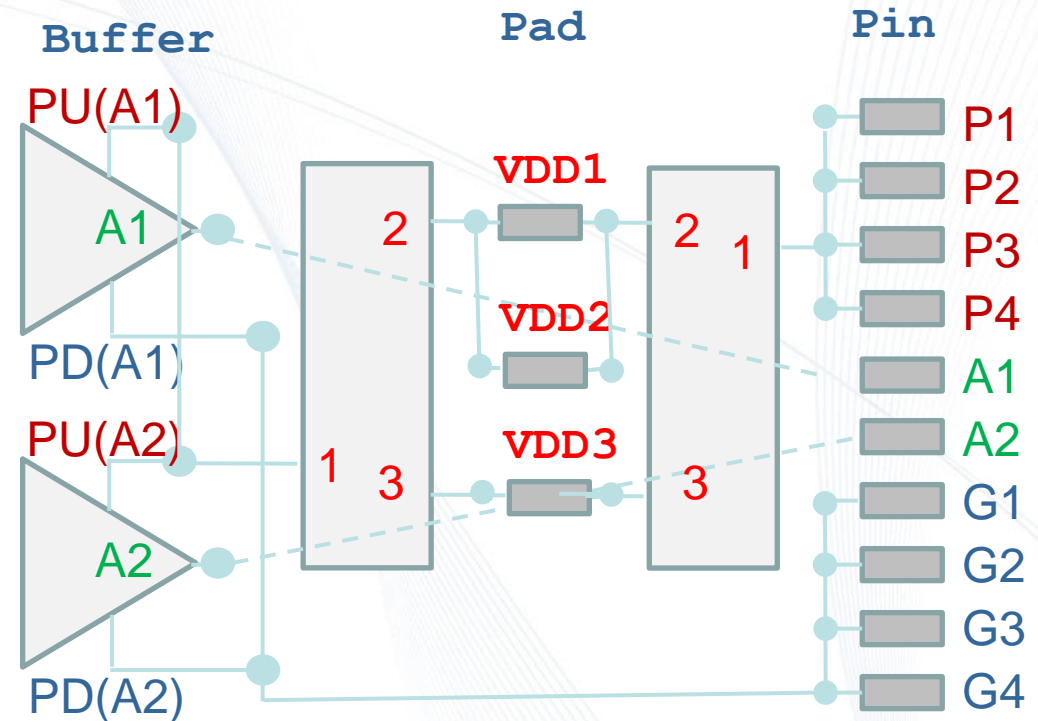
```
[Pin]      signal_name  model_name
A1         DQ1          DQ
A2         DQ2          DQ
P1         VDD          POWER
P2         VDD          POWER
P3         VDD          POWER
P4         VDD          POWER
G1         VSS          GND
G2         VSS          GND
G3         VSS          GND
G4         VSS          GND

[Pin Mapping] pulldown_ref pullup_ref
Bus_label_signal name
A1            VSS          VDD
A2            VSS          VDD

[Die Supply Pads] signal_name bus_label
VDD1           VDD          VDDa
VDD2           VDD          VDDa
VDD3           VDD          VDDb
[End Die Supply Pads]

[Begin Interconnect Model]
...
1 Pin_rail     signal_name  VDD
2 Pad_rail     bus_label    VDDa
3 Pad_rail     bus_label    VDDb
[End Interconnect Model]

[Begin Interconnect Model]
...
1 Buffer_rail  signal_name  VDD
1 Pin_rail    signal_name  VDD
2 Pad_rail    bus_label    VDDa
3 Pad_rail    bus_label    VDDb
[End Interconnect Model]
```



```
.subckt VDDPin2Pad_b1 1 2 3
.subckt VDDBuf2Pad_b1 1 2 3
XPinPad VDDPin VDDa VDDb VDDPin2Pad_b1
XBufPad VDDBuf VDDa VDDb VDDBuf2Pad_b1
```

Thank You

IBIS Interconnect Task Group

http://ibis.org/interconnect_wip/