

# Achieving Full System Signal Integrity for High Speed Backplane System

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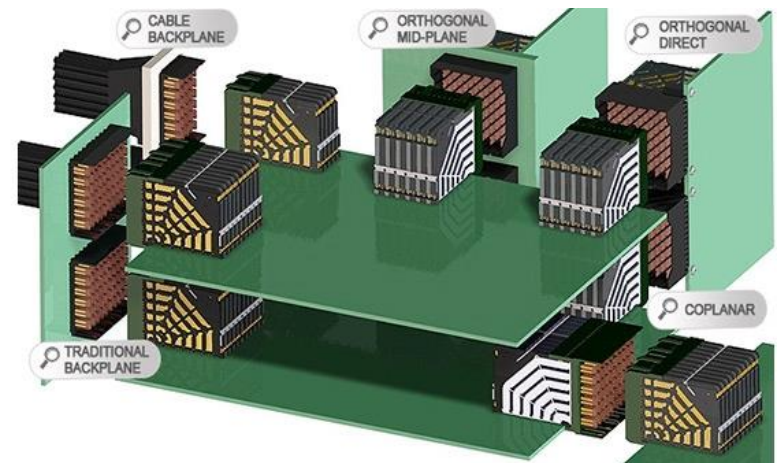


# Outline

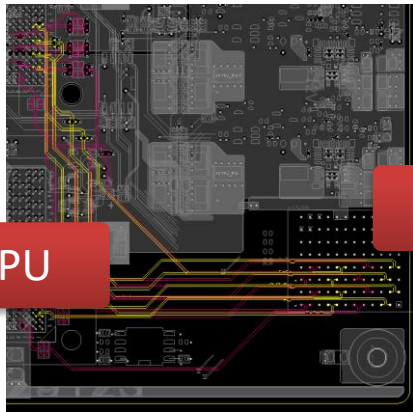
- Introduction of backplane system
- Challenge to backplane system simulation
- Components of EM simulation
- Analysis workflow
- Full backplane system SI simulation
- Summary

# Backplane System

- Backplane system is used as a backbone to connect several printed circuit boards together to make up a complete system
- There are various configurations
  - Traditional backplane
  - Orthogonal direct
  - Orthogonal mid-plane
  - Coplanar
  - Cable backplane

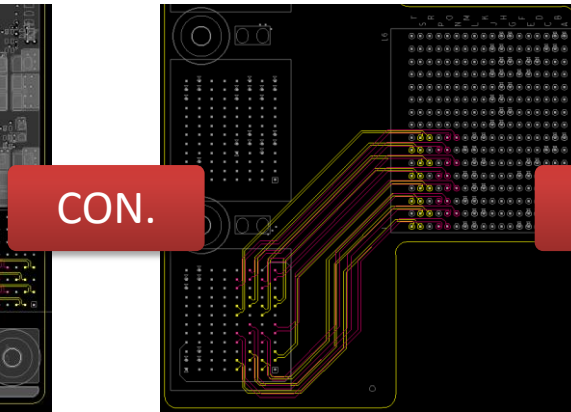


# Backplane System Example -- Server Board



CPU

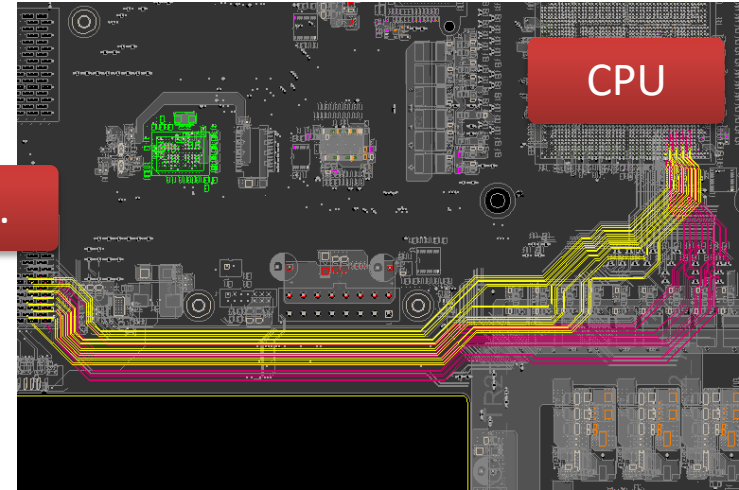
**CPU Board**



CON.

CON.

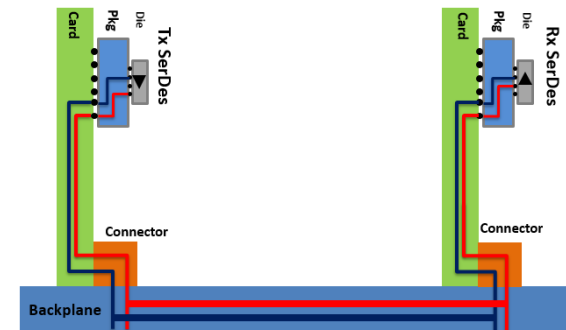
**Backplane**



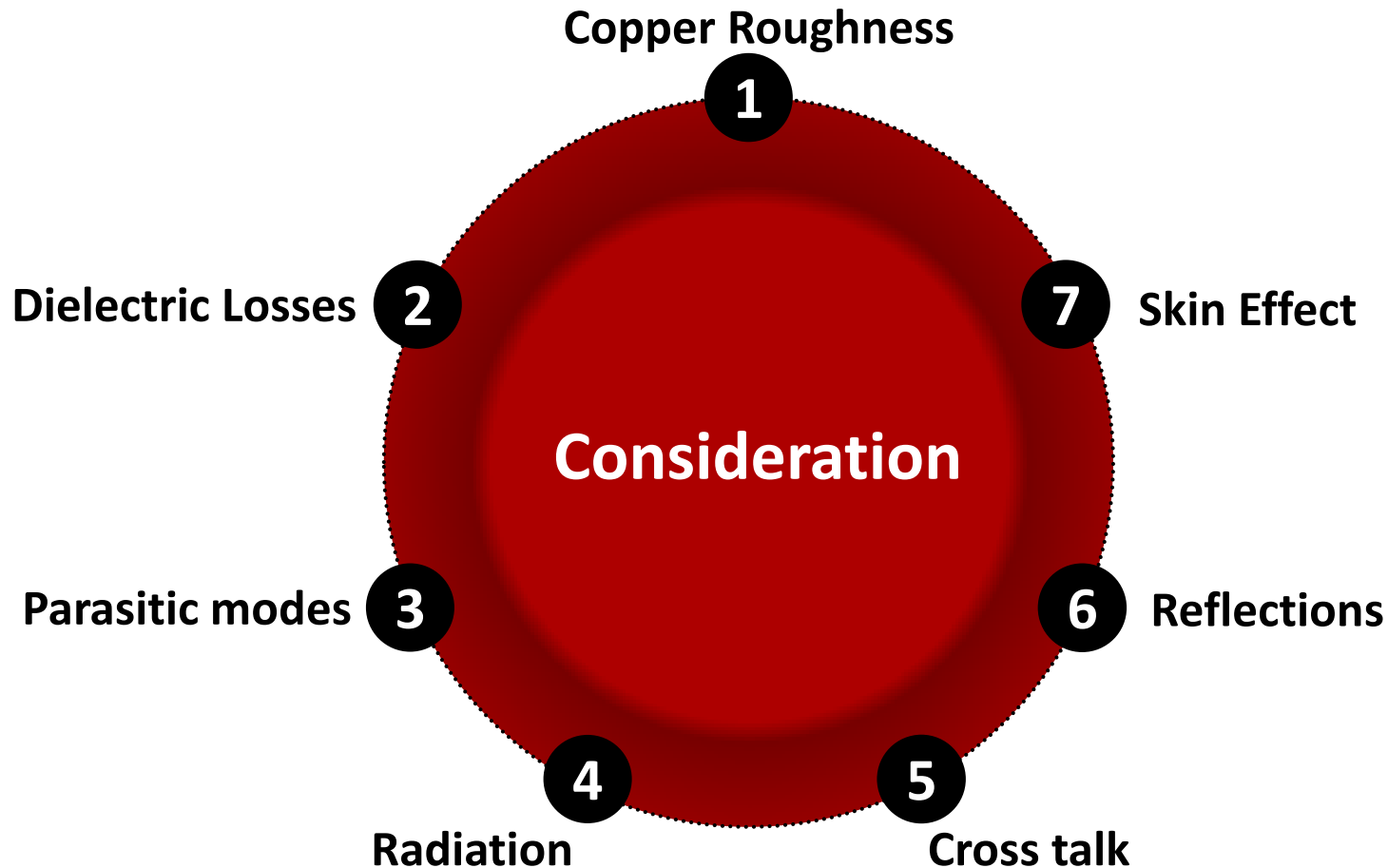
CPU

**Switch Board**

- Complex PCB layout.
- Maybe system has capacitor or repeater, Engineer need to check repeater gain based on channel's loss.



# Backplane Design Consideration

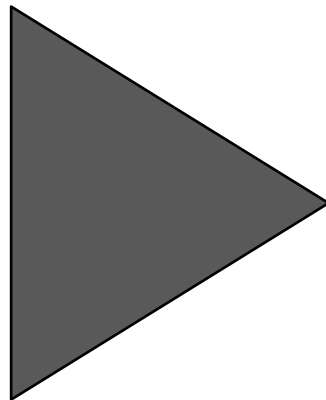


# Challenges to Channel SI Simulation

- Reflection noise due to impedance mismatch, via, connector and other discontinuities.
- Need to capture all physical parasitic effects
  - Reflection, Coupling, Delay, Freq. dependent Losses,...
- Measurements become very difficult,
  - Parasitic values are small but important at high speed.
  - Large number of ports for interconnects.
- EM simulation of the discontinuities is a must. However, the current flow suffers the following problems:
  - Manual process to extract the via, trace, and other discontinuities
  - Manual process to build all the channels

# Components of EM Simulation

✓ Transmitter



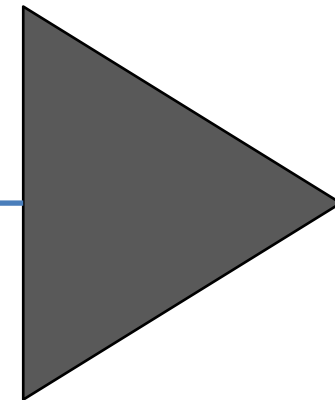
- Transistors
- Sources
- Algorithms
- Passives
- Memory

✓ Interconnect



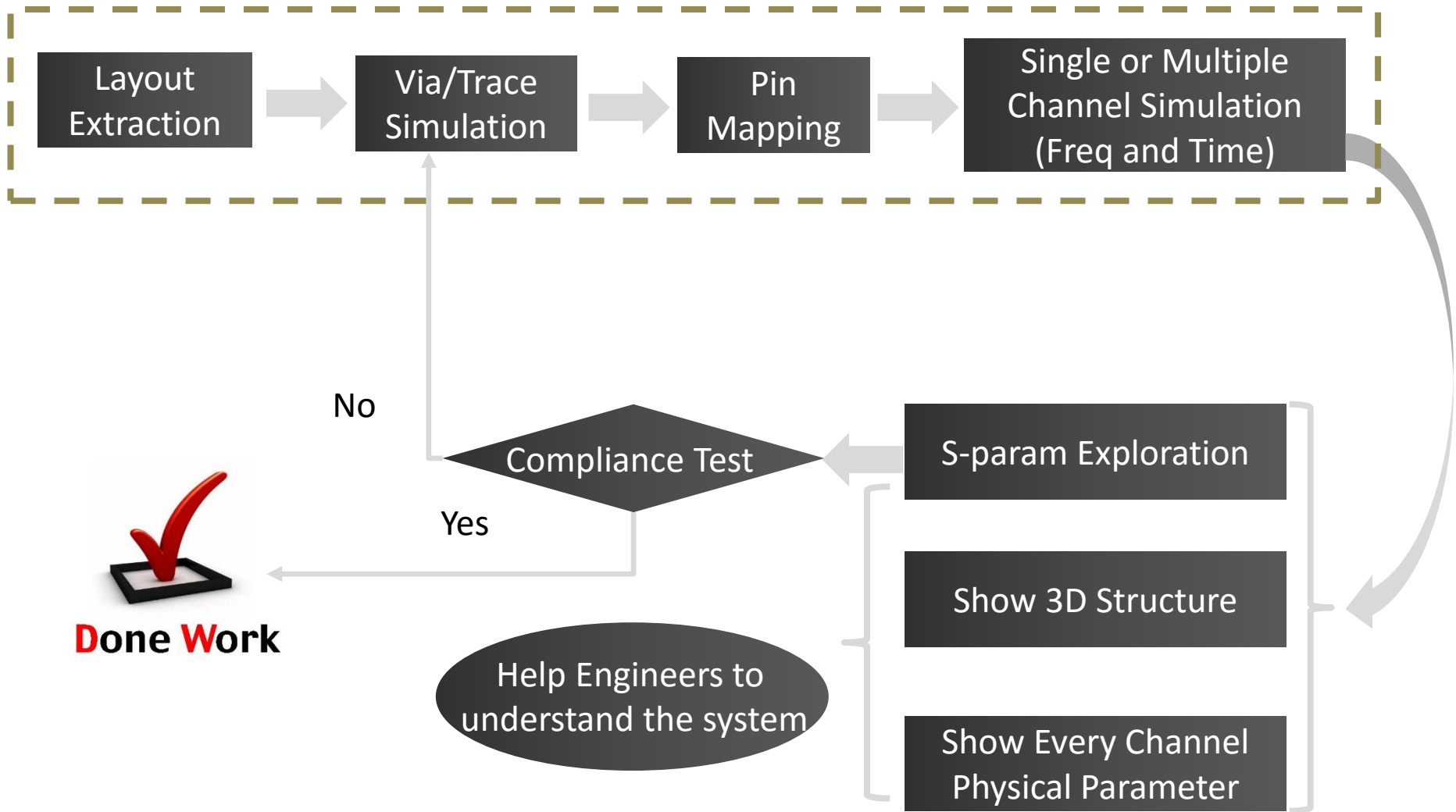
- **Thru Via**
- **BB Via**
- **Microstrip**
- **Stripline**
- **Capacitor**
- **Repeater**
- **Connector**
- **Backdrill**

✓ Receiver

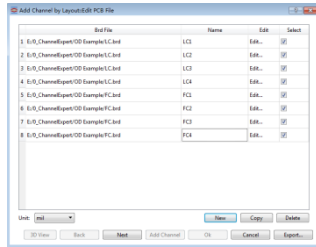


- Transistors
- Sources
- Passives
- Memory

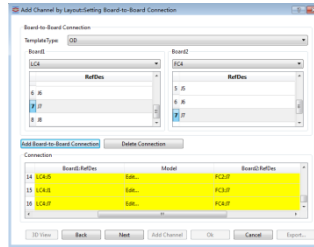
# Analysis Workflow



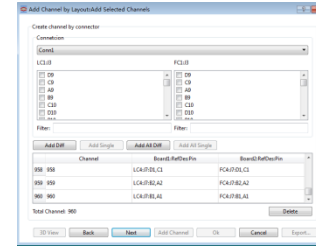
# Analysis Workflow



**Import  
Layout File**



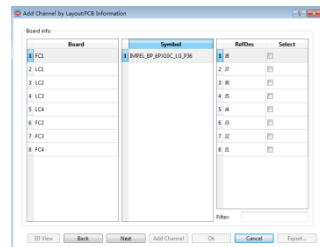
**Setting  
Connection**



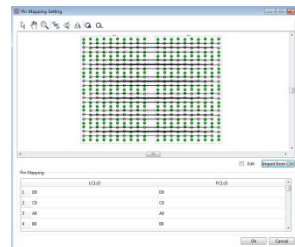
**Choose  
Channel**



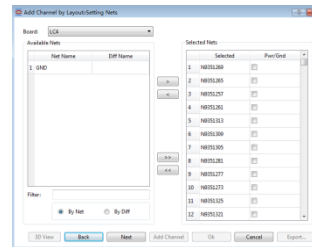
**Layout  
Information**



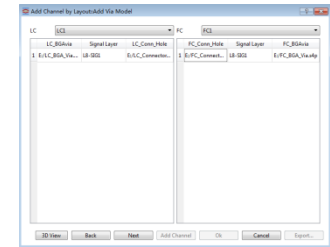
**Auto  
Pin Mapping**



**Choose  
Desired Net**



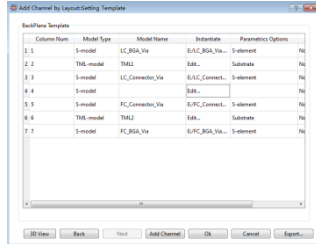
**Setting  
Via Model**



**Seamless Integration**

**Friendly User Interface**

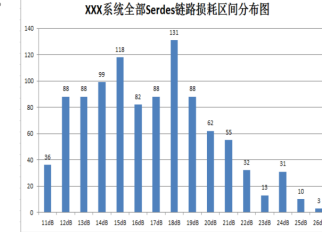
# Analysis Workflow



● **Create Channel Table**

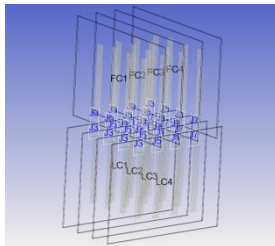


● **Create Excel File**

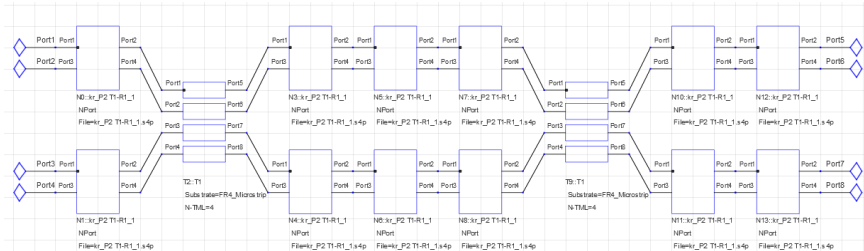


● **Batch Simulation**

● **Create 3D View**



● **Create Schematic**

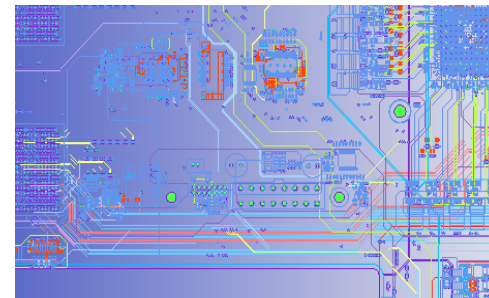
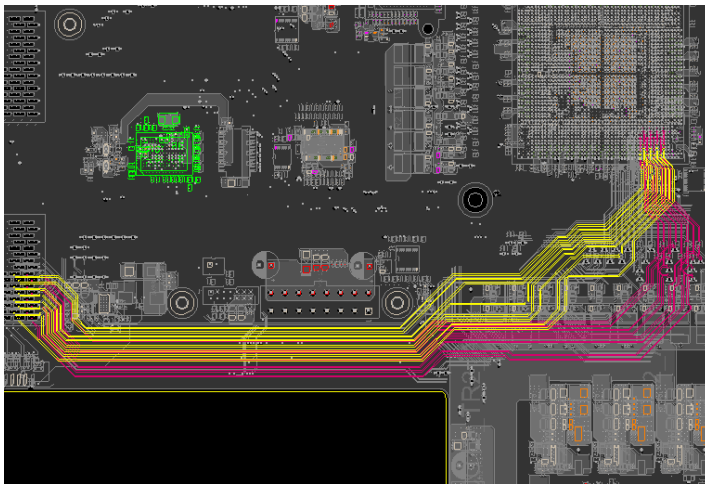


**Time and frequency domain solutions**

S-parameter, Crosstalk analysis, TDR, Eye diagrams

# Post-Layout Extraction

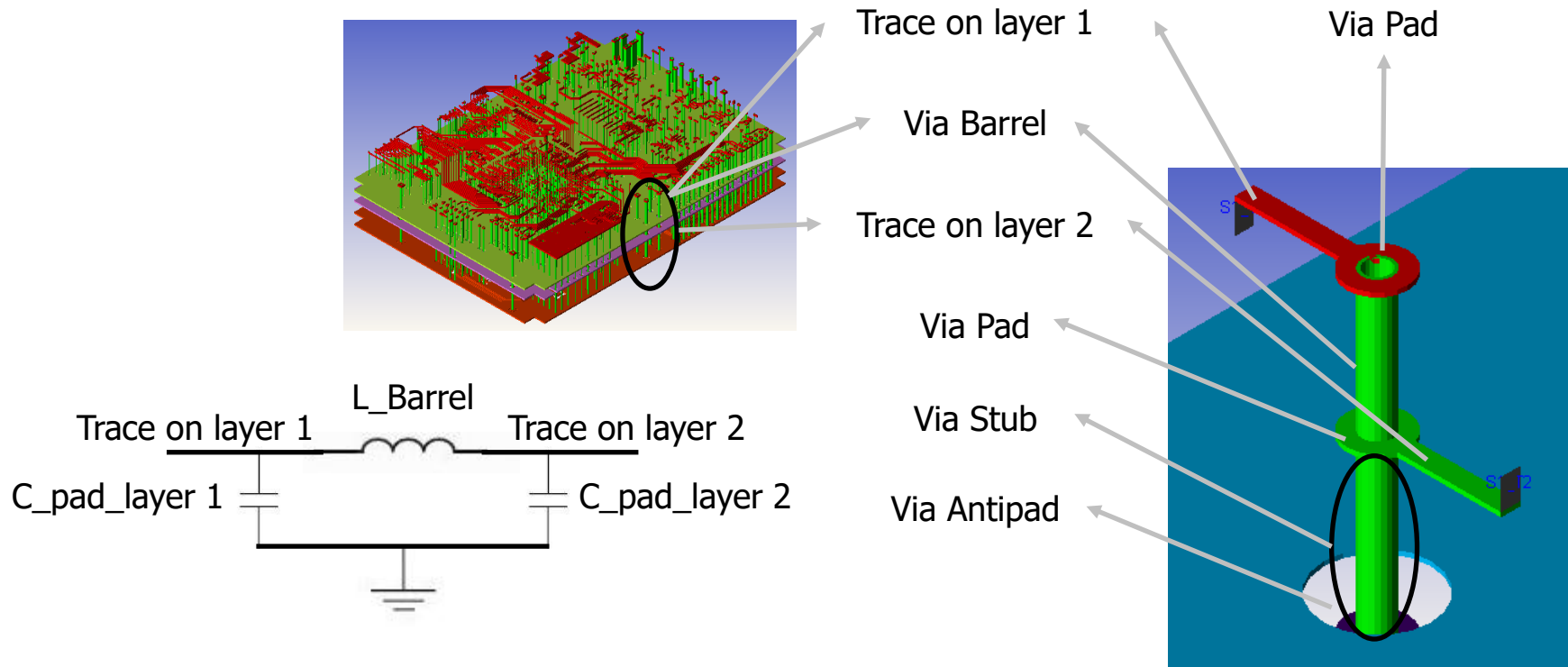
- Import all the boards for the backplane system
- Extract vias and traces from layout



- Layout Files
- Model Template

- Self cleaning process
- Discrete components
- Area/Net selection
- Stackup definition
- Materials definition
- BB, Back drill definition
- Auto port definition
- Parameter/Optimization
- High flexibility

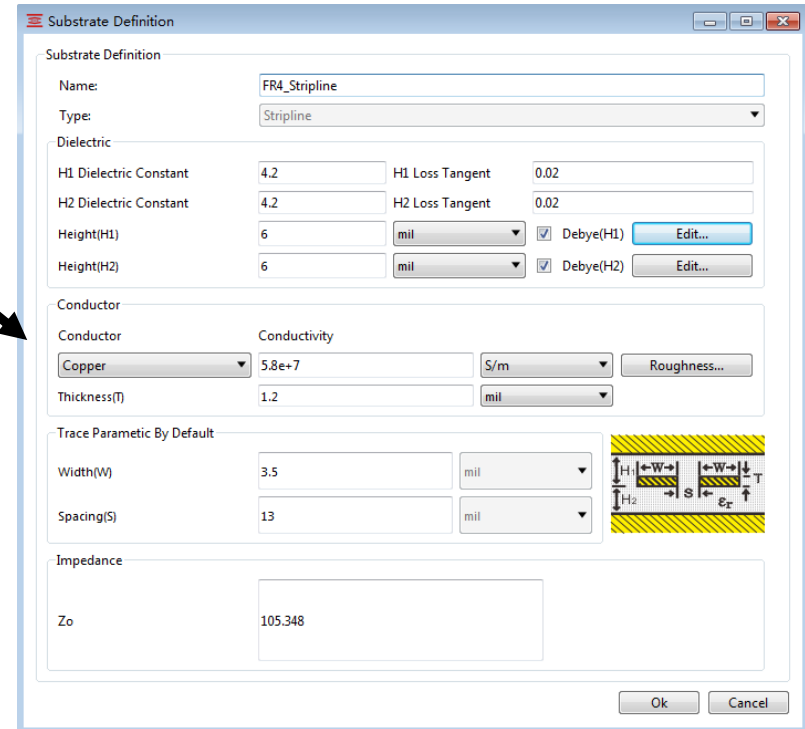
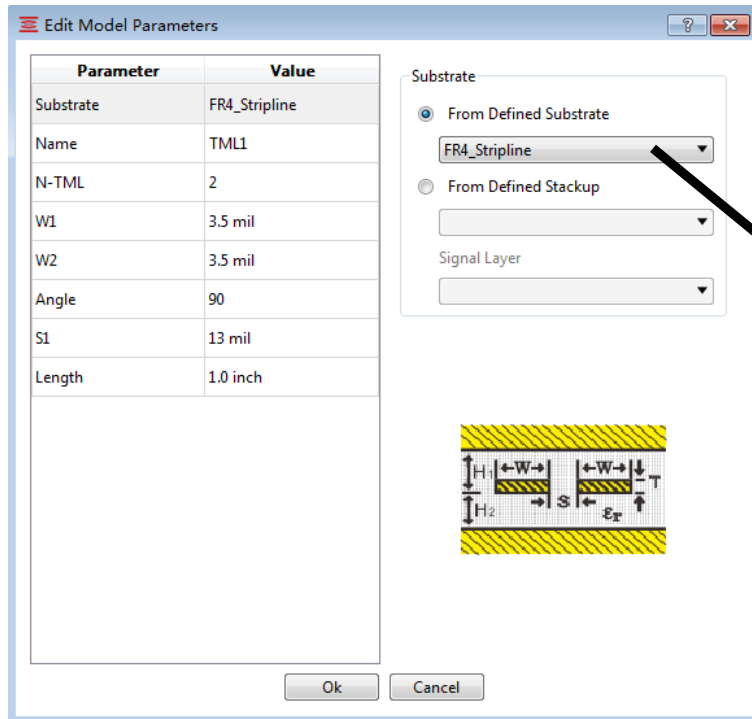
# 3D Via Modeling



- Via and ground plane will lead to **parasitic capacitance** and **parasitic inductance**.
- ***How to deal with a lot of via models?***

# Trace Modeling

- For trace, the common approach is to use 2D models for main high speed interconnect.



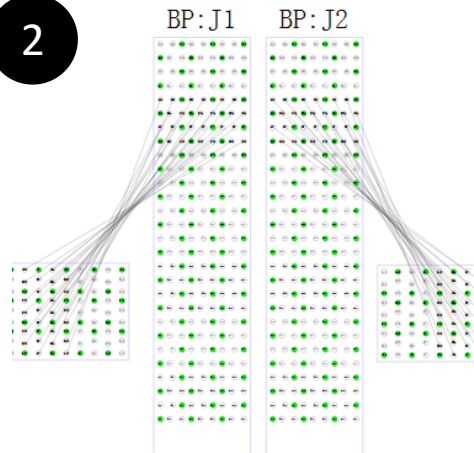
# Connection between Boards through Pin Mapping

1

	DC1:J1	BP:J1	Net	BP:J2	DC2:J1
1	A5	A5	W30...	A5	A5
2	A7	A7	W30...	A7	A7
3	B5	B5	W30...	B5	B5
4	B6	B6	W30...	B6	B6
5	B7	B7	W30...	B7	B7
6	B8	B8	W30...	B8	B8
7	C6	C6	W30...	C6	C6
8	C8	C8	W30...	C8	C8
9	D5	D5	W30...	D5	D5
10	D7	D7	W30...	D7	D7

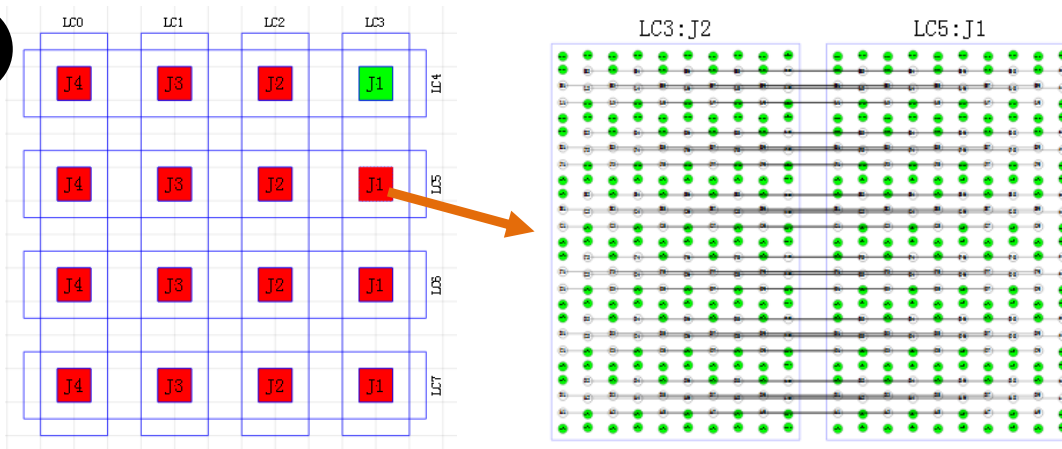
Edit

2

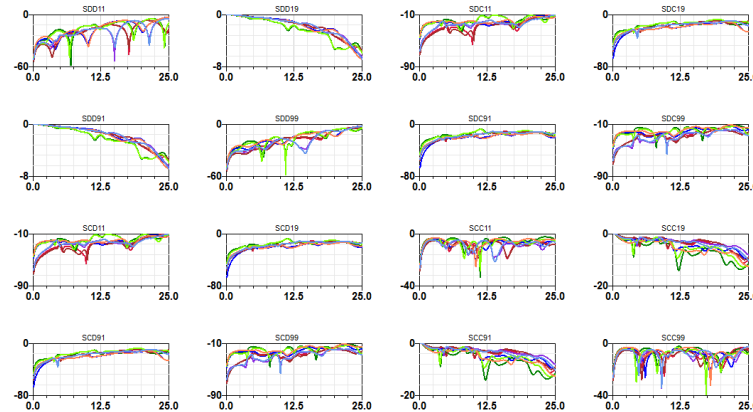
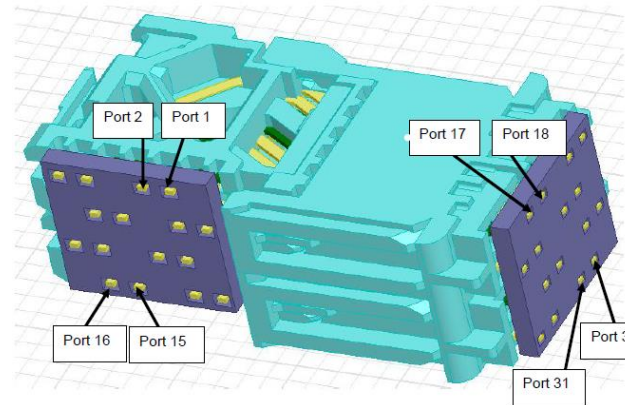
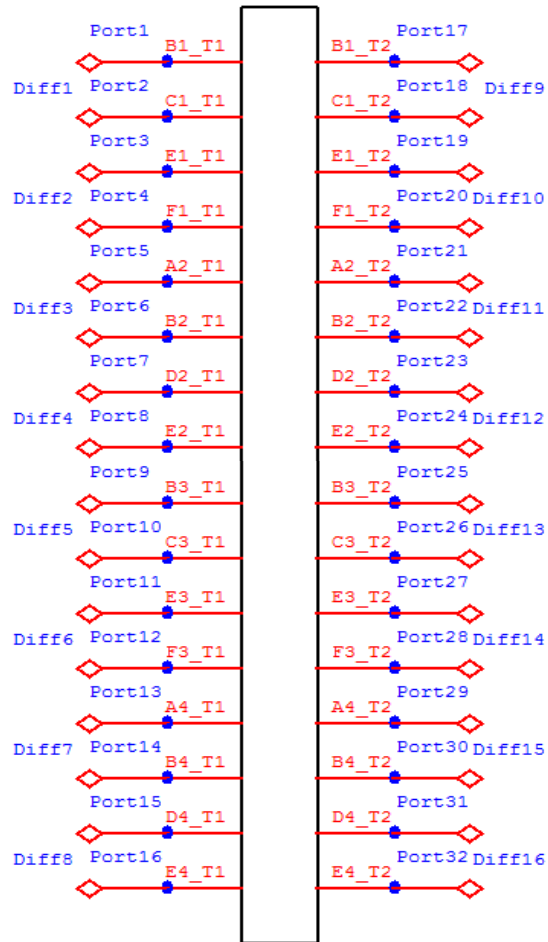


- Import .csv file.
- Create connection manually
- Create connection base on slot ID.

3

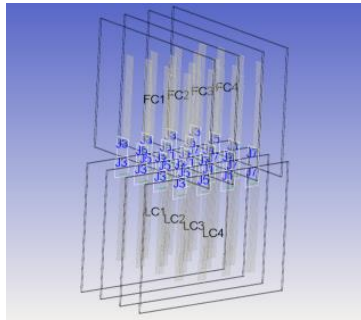


# Connector S-parameter from Vendor

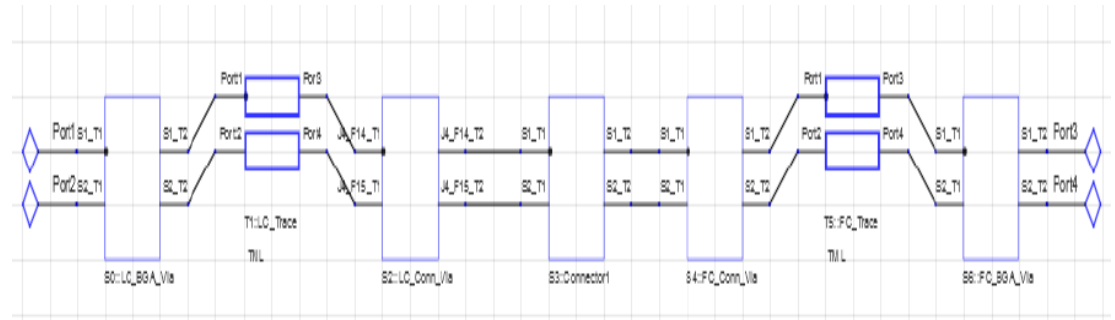


- Connector S-parameter file comes from vendor

# Auto Cascading to Create Channel



**Channelview**



**Cascading**

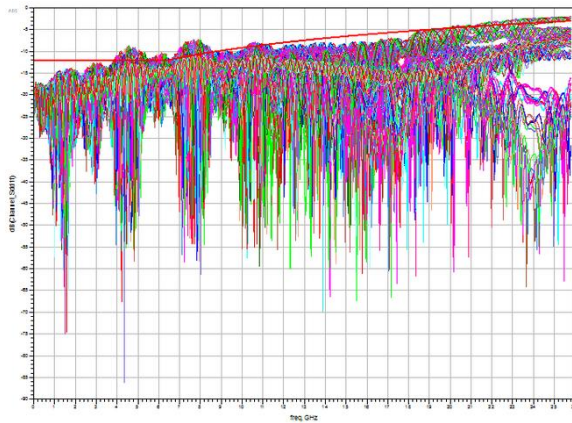
LC_Design	LC_Diff	LC_BGA_VIA	LC_Stackup	LC_layer	LC_Length	LC_DiffLine	LC_WDiffLine	LC_CONN_VIA	Connector	FC_Design	FC_CONN_VIA	FC_Diff	FC_Stackup	FC_layer	FC_Length	FC_DiffLine	FC_WDiffLine	FC_BGA_VIA	Total Length
LC0	0_Net1P/LC0_Net1	E:\democase\antipad	LC0_Stackup	L8	1000	5	4	E:\democase\antipad	E:\democase\antipad	FC0	E:\democase\antipad	CO_Net1P/FC0_Net1	FC0_Stackup	L2	2000	6	5	E:\democase\antipad	3000
LC1	0_Net2P/LC0_Net2	E:\democase\antipad	LC1_Stackup	L8	1500	5	4	E:\democase\antipad	E:\democase\antipad	FC1	E:\democase\antipad	CO_Net2P/FC0_Net2	FC1_Stackup	L6	3000	6	5	E:\democase\antipad	4500
LC2	0_Net3P/LC0_Net3	E:\democase\antipad	LC2_Stackup	L8	1500	5	4	E:\democase\antipad	E:\democase\antipad	FC2	E:\democase\antipad	CO_Net3P/FC0_Net3	FC2_Stackup	L6	3000	6	5	E:\democase\antipad	4500
LC3	0_Net4P/LC0_Net4	E:\democase\antipad	LC3_Stackup	L8	1500	5	4	E:\democase\antipad	E:\democase\antipad	FC3	E:\democase\antipad	CO_Net4P/FC0_Net4	FC3_Stackup	L6	3000	6	5	E:\democase\antipad	4500
LC4	0_Net5P/LC0_Net5	E:\democase\antipad	LC4_Stackup	L8	1500	5	4	E:\democase\antipad	E:\democase\antipad	FC4	E:\democase\antipad	CO_Net5P/FC0_Net5	FC4_Stackup	L6	3000	6	5	E:\democase\antipad	4500
LC5	0_Net6P/LC0_Net6	E:\democase\antipad	LC5_Stackup	L8	1500	5	4	E:\democase\antipad	E:\democase\antipad	FC5	E:\democase\antipad	CO_Net6P/FC0_Net6	FC5_Stackup	L6	3000	6	5	E:\democase\antipad	4500
LC6	0_Net7P/LC0_Net7	E:\democase\antipad	LC6_Stackup	L8	1500	5	4	E:\democase\antipad	E:\democase\antipad	FC6	E:\democase\antipad	CO_Net7P/FC0_Net7	FC6_Stackup	L6	3000	6	5	E:\democase\antipad	4500
LC7	0_Net8P/LC0_Net8	E:\democase\antipad	LC7_Stackup	L8	1500	5	4	E:\democase\antipad	E:\democase\antipad	FC7	E:\democase\antipad	CO_Net8P/FC0_Net8	FC7_Stackup	L6	3000	6	5	E:\democase\antipad	4500

## Excel File

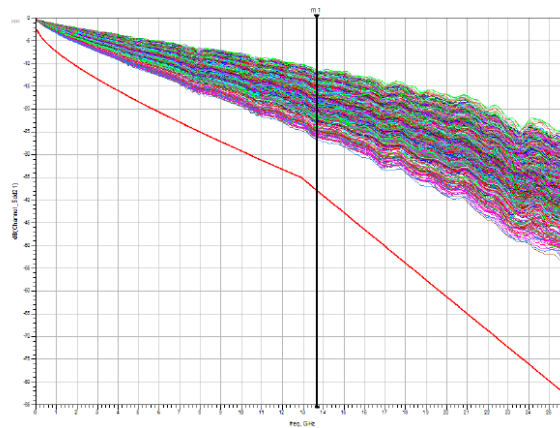
- 3D structure of BP system
- Hide/Show board or net in 3D
- Show entire channel path
- Single vs. multiple simulation and cascading
- Fast and memory efficient
- Show channel's structure size in Excel file
- Easily find worst channel
- Easily generate Excel report

# Full Backplane SI Simulation - Frequency Domain

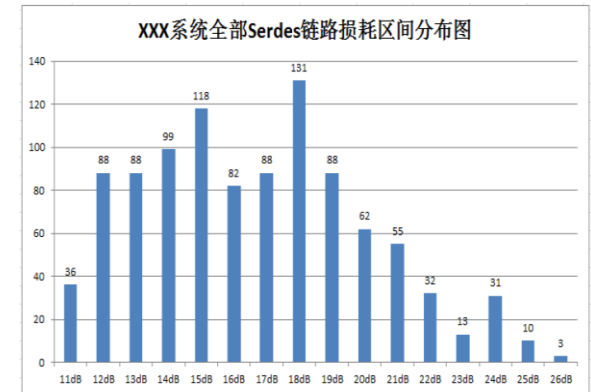
- Full backplane SI simulation is achieved by sweeping all the channels



Full Net Return Loss

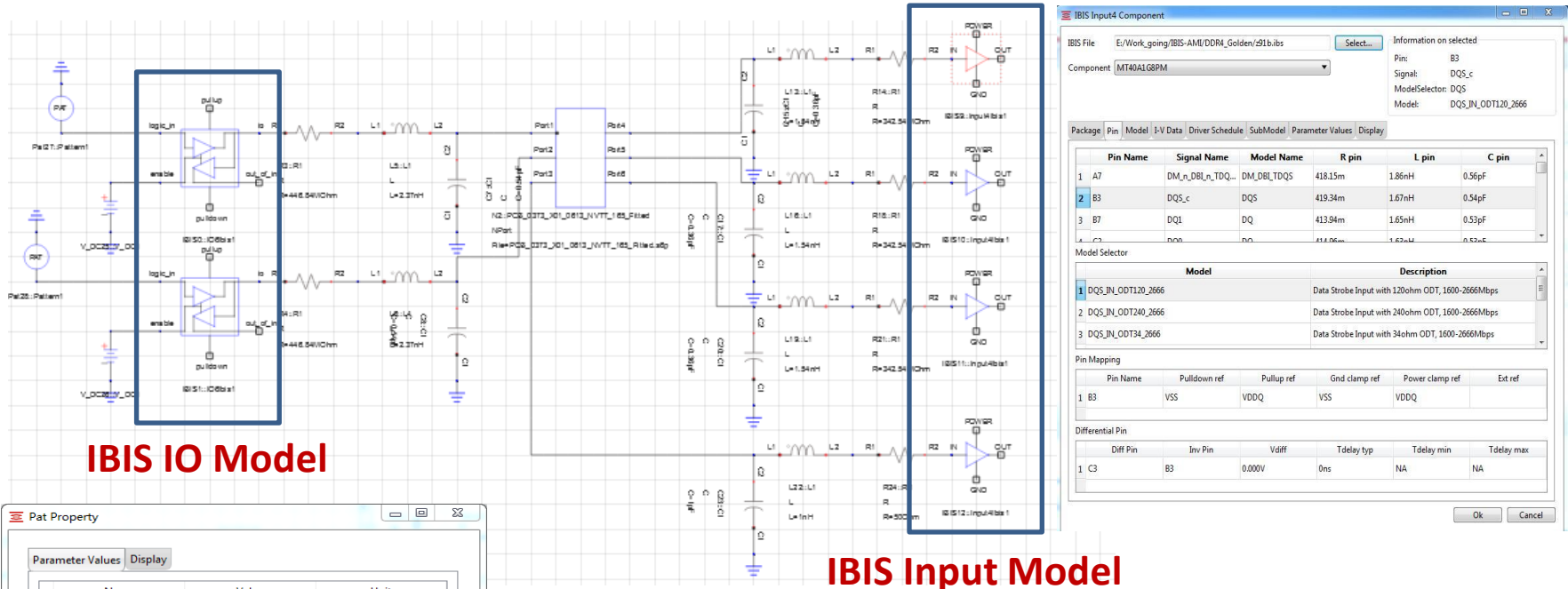


Full Net Insertion Loss



Net Distribution @ 13.67 GHz

# Full Backplane SI Simulation - Time Domain



**IBIS IO Model**

**IBIS Input Model**

Pat Property

Parameter Values Display

Name	Value	Unit
1 Vhi	1	v
2 Vlo	-1	v
3 Td	0	ns
4 Tr	1	ns
5 Tf	1	ns
6 Tsample	5	ns
7 Data	b0111001101100110	Binary
8 RB	1	
9 R	1	

Ok Cancel

IBIS Input4 Component

IBIS File: E:\Work\_going\IBIS-AMI\DDR4\_Golden\91b.ibs

Component: MT40A168PM

Information on selected:

Pin: B3  
Signal: DQS\_c  
ModelSelector: DQS  
Model: DQS\_IN\_ODT120\_2666

Package Pin Model I-V Data Driver Schedule SubModel Parameter Values Display

Pin Name	Signal Name	Model Name	R pin	L pin	C pin
1 A7	DM_n_DBL_n_TDQ...	DM_DBL_TDQS	418.15m	1.86nH	0.56pF
2 B3	DQS_c	DQS	419.34m	1.67nH	0.54pF
3 B7	DQL	DQ	413.94m	1.65nH	0.53pF
4 C3	non	no	414.06m	1.63nH	0.63pF

Model Selector

Model	Description
1 DQS_IN_ODT120_2666	Data Strobe Input with 120ohm ODT, 1600-2666Mbps
2 DQS_IN_ODT240_2666	Data Strobe Input with 240ohm ODT, 1600-2666Mbps
3 DQS_IN_ODT34_2666	Data Strobe Input with 34ohm ODT, 1600-2666Mbps

Pin Mapping

Pin Name	Pulldown ref	Pullup ref	Gnd clamp ref	Power clamp ref	Ext ref
1 B3	VSS	VDDQ	VSS	VDDQ	

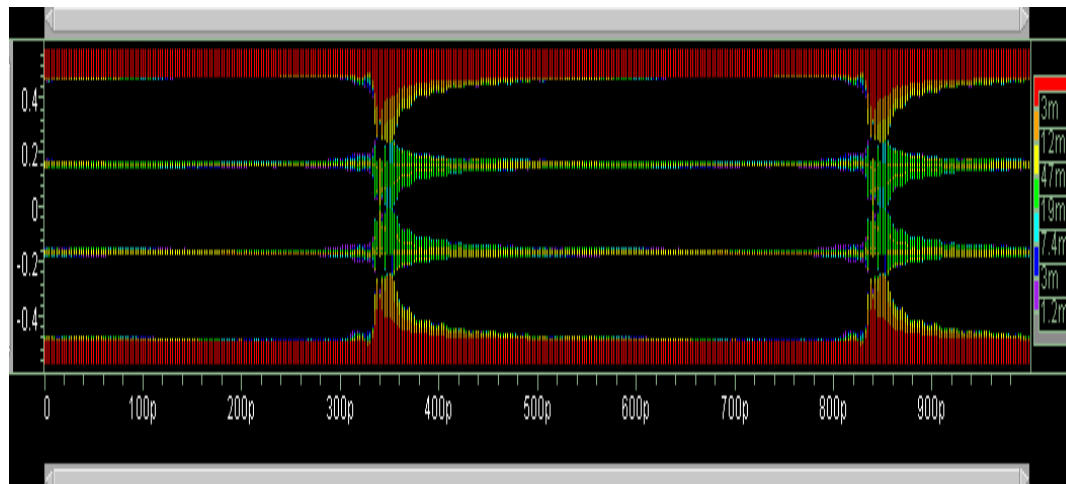
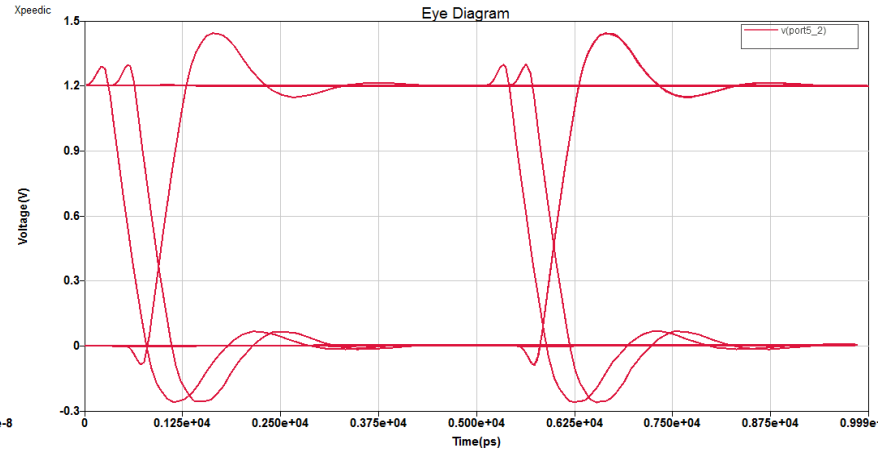
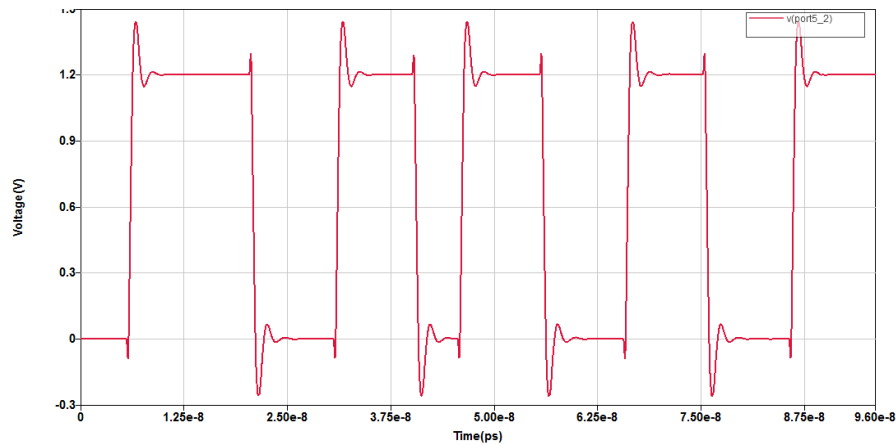
Differential Pin

Diff Pin	Inv Pin	Vdiff	Tdelay typ	Tdelay min	Tdelay max
1 C3	B3	0.000V	0ns	NA	NA

Ok Cancel

- Support IBIS, IBIS-AMI, Spice model.
- Add proper pattern model.
- Fast modeling and high accuracy.

# Full Backplane SI Simulation - Time Domain



# Summary

- Passive channel modeling and simulation is essential to high speed channel design.
- Optimal channel design requires user friendly EDA tool to do layout extraction, via optimization, trace simulation, S-parameter cascading, S-parameter exploration, etc.
- Full backplane system SI simulation is achieved by sweeping all the channels with correct models.

**XPEEDIC**  
ACCELERATE YOUR IC DESIGN