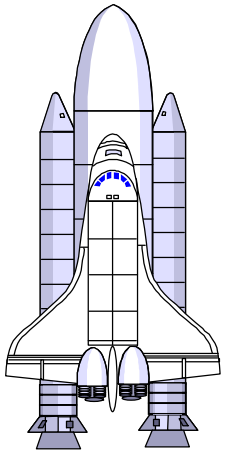
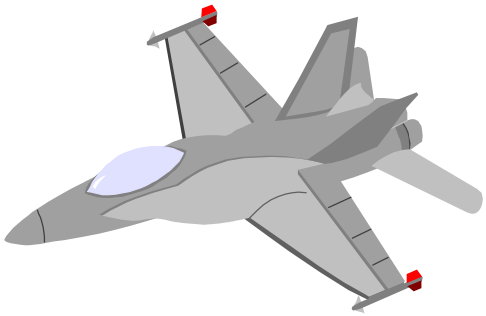
Die Information Exchange (DIE) Format



IBIS Open Forum Summit
12 Nov 1993



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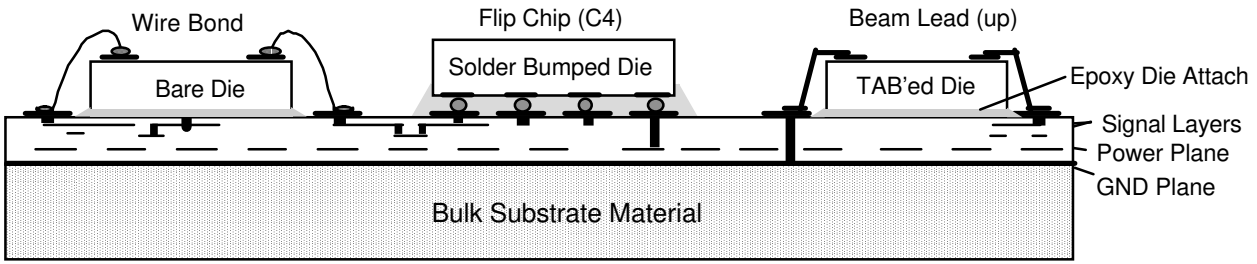
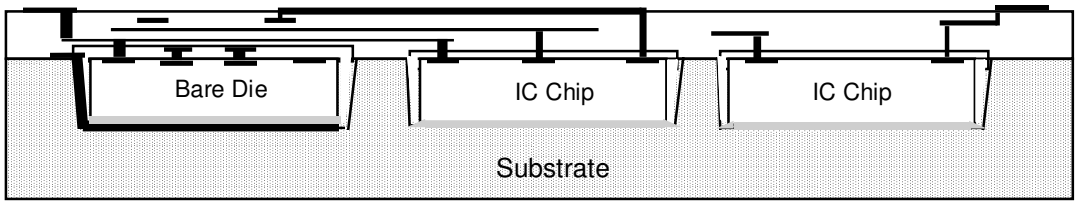
Example MCM Processes and Die Use



MCM-D Shown (only substrate different from MCM-C)



hips first (High Density Interconnect)

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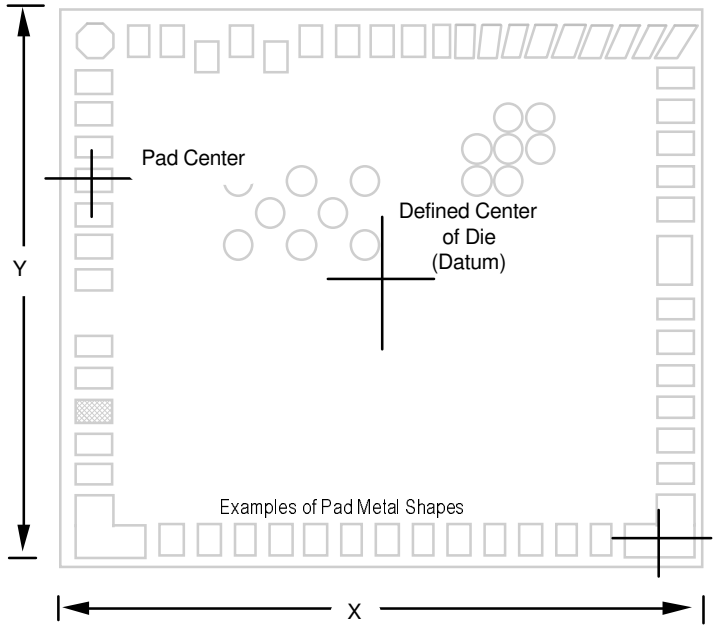
Example Die Bonding Diagram
(sample die pad examples)



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Die (Device) Information Exchange (DIE)
Format (version 0.9)

- **Computer / EDA tool sensible and human sensible (EDA as much as possible)**
- **Going for complete linear EDB (in CFI CIR terminology)**
- **Have today:**
  - **administration, geometrical, material, thermal, AC/DC signal, power, noise, conditions**
  - **Bare die**
- **Soon:**
  - **timing, test (BSDL), behavioral model**
  - **Flip chip, Beam lead specifics (geometrical; electrical differences) (many hooks; should not be much additional effort to add)**
- **Not planned (yet?):**
  - **quality / KGD issues; speed sort identification**
  - **Passives, Discretes**

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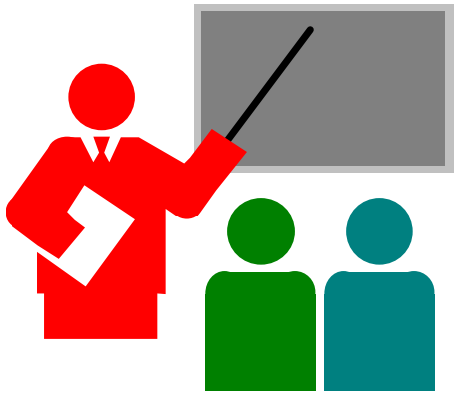
Status

- **Completed studies**
- **Held two physical die information workshops**
- **DIE Format 0.9 Draft out**
  Rigorous spec on format with BNF, examples, and justification
- **Receiving broad industry interest**
- **DIE Draft 0.9 covers admin., material, geometrical, electrical, thermal, and power completely.**
- **DIE Draft x.x to cover behavioral / functional, timing, and test (additional constructs)**



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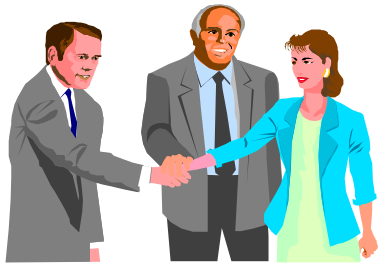
Industry Cooperation

- **MCM Foundries**
  IBM, Motorola, nCHIP, TI, Hughes, National Semiconductor, *MMS*
- **EDA MCM Vendors**
  Mentor Graphics, Harris EDA, Intergraph, *Cadence, Racal Redac*

  Pacific Numerics, Quad Design, IBIS Open Forum



- **Bare Die Vendors:** National Semiconductor, Intel, Micron, IDT, Motorola, Texas Instruments

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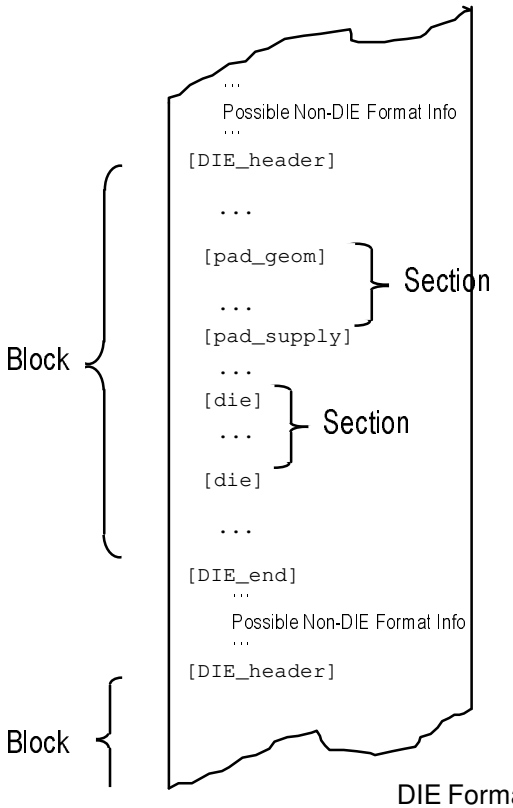
DIE Linear / Transport EDB

- **Can embed Die information in DIE block**
- **Like waffle pack -- purely a convenient carrier**
- **Allows libraries of common definitions independent of specific Die and electrical pad (port, pin, pad) instance**
- **Currently, unique new syntax. Considering SGML derivative without forcing SGML knowledge**



DIE Format (v0.9)
Page 8

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DIE Format Structure

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3.2.	Comments	18
3.3.	Tokens	18
3.4.	Keywords	18
3.5.	Values	19

- ➡ **Content Name Tag (begin/end)**
- ➡ **Content Name Tag (begin only)**
- ➡ **Content Name Tag (begin/end)**
- ➡ **Not Tagged (positional assoc)**

- ***Proposal to change block and sections to SGML <key>, </key> tagging***
- ***Proposal to change setting to SGML <key> tagging***
- ***Proposal to add optional tagging to attributes***

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Sections

Main Buckets of Information

- **Types:**
  - **Primary**
    - » **(Bare) Die, *Flip Die, TAB Die, Discrete, Passive***
  - **Definition**
    - » **Pad Geometry, Pad (signal) Digital, Pad Supply, *Pad (signal) Analog***
  - **Secondary**
    - » **Wafer, Die (Lot) Measure**
  - **External Models**
    - » **IBIS, *VHDL, BSDL, WAVES/SVF, EDIF Symbol(s)***
- **Uniquely named (ID, Name), version controlled (primary)**

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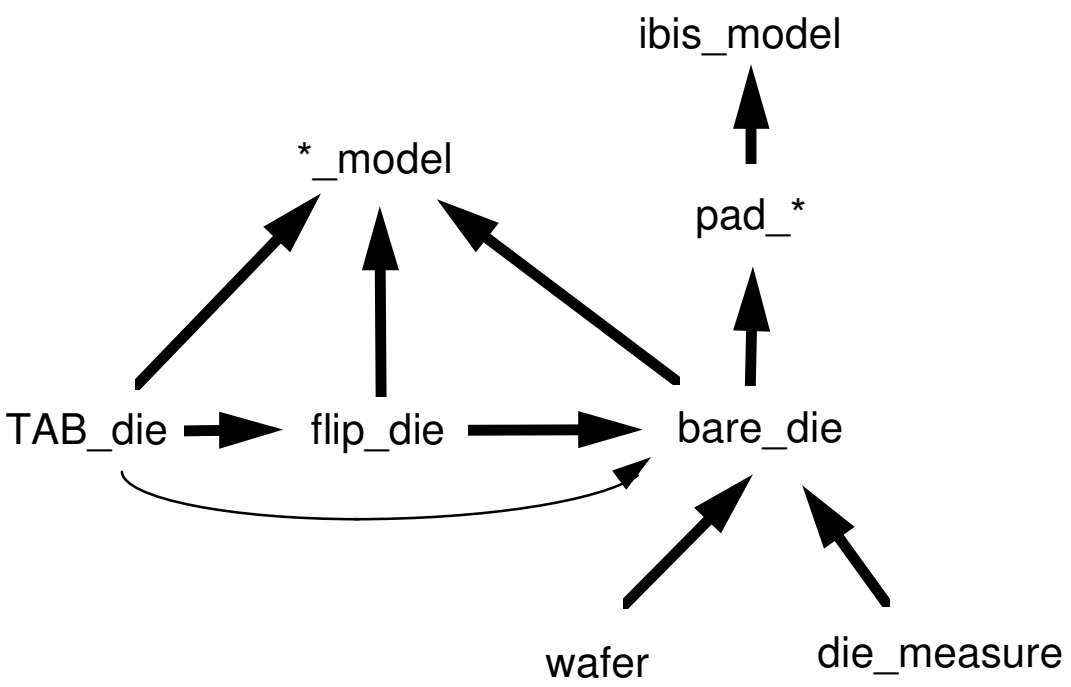
Section Referencing



* is a wild card match which represents all similar sections not listed

— represents a direct reference

B references A

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Settings

Main Information Carriers

- **82+ settings (expect 100+ by 1Q94)**
- **Simple (single value from list) to complex (die_pads instance list)**
- **Introduction of Compliance Levels:**
  - **Level 0: Minimum; all blocks must have**
  - **Level 1: Should have; newly developed or difficult to backfill**
  - **Level 2: Very specialized; only delivered if NDA or convenient.**
- **Includes model references and port maps**
- **Collection of related information**

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Bare Die - Level 0 Settings

Setting Keyword	Description	Key
die_ID	Unique ID (at least in the block) assigned to the die	pri
die_name	Manufacturers published name for die	sec
die_manufacturer	Manufacturer's name	sec
die_mask_version	Manufacturers published mask step version of die	sec
die_junction_temperature	Recommended operating die junction temperature	
die_power_max	Maximum die power dissipation	
die_power_nom	Nominal die power dissipation	
die_packaged_part_name	Name(s) of conventionally packaged components which use this die.	
die_pads	Instances of pads for die	
die_section_version	Version of die information provided in this section	
die_size	Die width and height	
die_source	Source of information about the die.	
die_substrate_connection	Electrical connection of the die substrate.	
die_substrate_material	Bulk substrate material of the die	
die_technology	Manufacturer published process name / technology of the die	
die_thickness	Thickness of die (Z dimension)	

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Bare Die - Level 1 Settings

Setting keyword	Description
die_backside_finish	Die backside finish and optional coating material list
die_bonding_diagram	Reference to available bonding diagram or description
die_conditions_storage	Suggested not to exceed conditions for storage.
die_packaged_part_bonding	Pad bonding methods used for packaged or TAB delivered die
die_pad_pitch	Minimum center-to-center spacing of pads on die
die_pads_supply_grouping	Supply pad groups
die_pads_tolerance	Tolerance of pad placement
die_passivation_material	Material of passivation layer outer coating
die_size_tolerance	Die width and height tolerance(s)
die_specific_heat_capacity	Specific heat capacity of the substrate material
die_thermal_conductivity	Thermal conductivity of the substrate material
die_thickness_tolerance	Tolerance of the die thickness

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Pad Digital - Level 0 and 1 Settings

Setting keyword	Description
pad_digital_name	Pad digital signal section name
pad_digital_circuit	Describes the pad circuit
pad_digital_pull_down	Pad output driving capability at logic low level
pad_digital_pull_up	Pad output driving capability at logic high level
pad_digital_threshold	Pad input switching characteristics
pad_digital_ibis_model	IBIS model reference

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Pad Supply - Level 0 and 1 Settings

Setting keyword	Description
pad_supply_name	Power supply section name
pad_supply_current_max	Maximum current limit
pad_supply_voltage	Supply voltage specification

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Die_pads Setting Definition
(SYNTAX ONLY)

4.41. die_pads

Instances of pads for die

Syntax

```
<die_pads> ::= die_pads <num_pads> <pad_descr_list> ';'
<num_pads> ::= <numeric_value>
<pad_descr_list> ::= <pad_descr> { ',' <pad_descr> }
<pad_descr> ::= <pad_ID> <pad_geom_inst> <pad_elec_inst> <pad_info>
<pad_ID> ::= <ID_value>
<pad_geom_inst> ::= <pad_geom_ref> <point> <rotmir>
<pad_geom_ref> ::= <name_value>
<pad_elec_inst> ::= <pad_type> [ <pad_elec_ref> ]
<pad_type> ::= supply_power | supply_ground | signal_digital |
                    signal_analog | test_point | no_connect | not_defined
<pad_elec_ref> ::= <name_value>
<pad_info> ::= [ <pad_common_name> [ <pad_swap_code> ] ]
<pad_common_name> ::= <name_value>
<pad_swap_code> ::= <swap_function> <pin_type> <pin_group>
<swap_funcion> ::= <numeric_value>
<pin_type> ::= <numeric_value>
<pin_group> ::= <numeric_value>
```


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Pad_digital_circuit Setting Definition
(SYNTAX ONLY)

4.65 Pad_Digital_Circuit

Describes the pad circuit

Syntax

```
<pad_digital_circuit> ::= pad_digital_circuit <technology> <type> ';'
<technology> ::= ECL | TTL | CMOS | NMOS | PMOS
<type> ::= [ input ] [ <active_driver> ] [ <passive_driver> ]
<active_driver> ::= output | tristate | open_collector | open_emitter |
                    open_drain | open_source
<passive_driver> ::= pull_up | pull_down
```


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Bare Die - Level 2 Settings

Setting keyword	Description
die_bonding_sequence	Suggested sequence to bond pads
die_conditions_bonding	Suggested not to exceed conditions during single pad bonding (pad vicinity conditions)
die_conditions_process	Suggested not to exceed conditions for die attach processing.
die_conditions_sealing	Suggested not to exceed conditions for processing of die (vicinity conditions during sealing)
die_conditions_special	Any special conditions for handling or use of the die
die_description	Textual description of die features
die_flatness	Indication of die surface warpage
die_load_factor	Output load dependency of the die power dissipation.
die_lot	Lot number(s) of die this information pertains to.
die_military_spec	Military part specification, if it exists
die_manufacturer_cage	CAGE code of manufacturer
die_packaged_part_attach	Packaged part (and possibly TAB) methods of attaching bare die to carrier.
die_pad_dielectric	Dielectric material under the pads composition and thickness
die_pad_metal	Pad metal layer composition and thickness
die_passivation_extent_size	Extent of passivation if different from die size.
die_passivation_stack	Material list of all passivation layer coatings AND thicknesses
die_power_capacitance	Frequency dependency of the internal die power dissipation
die_power_cell	Nominal power dissipation of specific areas
die_quiescent_current	Quiescent current consumption
die_saw_step_error	Maximum saw or scribe step error during dicing
die_saw_width	Width of saw (cut), if die separated by saw

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DIE Format Example

(Block Header)

```
|
|-------------------------------------------------------------------------
-
|  block definition section
|-------------------------------------------------------------------------
-
|
[die_header]
|
block_die_format_version    0.9;
block_level         0;
|
block_version       1.0 4 Nov 93;
block_source        author: REH, Logic Modeling Corporation;
block_disclaimer
          These models are provided as a demonstration vehicle for
          the DIE draft version 0.9. LMC does not assume any
          liability arising out of the application and use of any
          information described herein.
          ;
block_notes   This block represents an example of DIE format version 0.9.
              There are three (3) die from three (3) different manufacturers.
              ;
```


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DIE Format Example

(NS 18245T Pad Geom)

```
|-------------------------------------------------------------------------
|         National Semiconductor SCAN 18245T MDA Bare Die
|-------------------------------------------------------------------------
|  pad geometry definition sections
|-------------------------------------------------------------------------
|
[pad_geom]
pad_geom_name           3_8milsquare;
pad_geom_shape          rectangle 3.8mil 3.8mil;
pad_geom_bond_sites     1 0.0mil 0.0mil;
                         | Single bond site at center of pad
|
[pad_geom]
pad_geom_name           3_8milwide;
pad_geom_shape          rectangle 3.8mil 8.08mil;
pad_geom_bond_sites     2 0.0mil 2.18mil 0.0mil -2.18mil;
                         | The National Semi data sheet specifies the
                         | center of two 3.8mil pads separated by
                         | 0.48mil.  It actually represents a single  pad.
|
```


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DIE Format Example

(pad_digital section examples)

```
|-------------------------------------------------------------------------
|  pad digital signal definition sections
|-------------------------------------------------------------------------
[pad_digital]
pad_digital_name cmos_input_pad;
pad_digital_circuit cmos input;
pad_digital_thresholds 2
                4.5V 2.0V 1.0uA 0.8V 1.0uA,
                5.5V 2.0V 1.0uA 0.8V 1.0uA;
pad_digital_ibis_model input1;
| ....
[pad_digital]
pad_digital_name cmos_output_pad;
pad_digital_circuit cmos output;
pad_digital_pull_down 4 4.5V  48mA 0.55V,| ....
                5.5V  50uA 0.1V;
pad_digital_pull_up   4 4.5V -24mA 2.4V, | ....
                5.5V -50uA 4.15;
pad_digital_ibis_model output1;
[pad_digital]
pad_digital_name cmos_io_pad;
pad_digital_circuit cmos input tristate;
pad_digital_thresholds 2 5.5V 2.0V 1.0uA 0.8V 1.0uA;
pad_digital_pull_down 2 4.5V  48mA 0.55V, 5.5V  63mA 0.55V;
pad_digital_pull_up   2 4.5V -24mA 2.4V,  5.5V -27mA 2.4V;
pad_digital_ibis_model transceiver;
|
```


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DIE Format Example

(pad_supply and die administration section example)

```
|-------------------------------------------------------------------------
| power supply pad definition sections
|-------------------------------------------------------------------------
[pad_supply]
pad_supply_name VCC_supply;
pad_supply_voltage fixed 5.0V 4.5V 5.5V;
pad_supply_current_max 70mA;
|
[pad_supply]
pad_supply_name GND_supply;
pad_supply_voltage fixed 0.0V 0.0V 0.0V;
pad_supply_current_max 70mA;
|
|-------------------------------------------------------------------------
|               die definition sections
|-------------------------------------------------------------------------
[die]
die_id                  1;
die_name                SCAN18245T-MDA;
die_manufacturer        National Semiconductor;
| die_mask_version      ; not found in the data sheet
die_section_version     1.1 29/10/92;
die_source              Information is taken from National Semiconductor
                        SCAN18245T MDA data sheet September 1993.;
```


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DIE Format Example

(Bare Die Pad List Example Setting)

```
die_pads 56
| pad    pad           pad center   rot     pad        electrical   pad   swap
| id   geometry        X       Y    mir     type       model        name  codes
| --   -----------  ------- ------- --- -------------- ------------ ----- -----
  1   3_8milsquare  -2025.1  1582.4   0 signal_digital cmos_io_pad  B1[4] 1 4 4,
  2   3_8milwide    -2025.1  1242.4   0 supply_power   VCC_supply   VCC   0 5 0,
  3   3_8milsquare  -2025.1   915.7   0 signal_digital cmos_io_pad  B1[5] 1 4 5,
  4   3_8milsquare  -2025.1   698.0   0 signal_digital cmos_io_pad  B1[6] 1 4 6,
  5   3_8milsquare  -2024.9   494.3   0 supply_ground  GND_supply   GND   0 6 0,
  6   3_8milsquare  -2025.1   256.3   0 signal_digital cmos_io_pad  B1[7] 1 4 7,
  7   3_8milsquare  -2025.1    87.9   0 signal_digital cmos_io_pad  B1[8] 1 4 8,
  8   3_8milsquare  -2025.1   -87.1   0 signal_digital cmos_io_pad  B2[0] 2 3 9,
  9   3_8milsquare  -2025.1  -255.5   0 signal_digital cmos_io_pad  B2[1] 2 3 1,
 10   3_8milsquare  -2024.9  -493.5   0 supply_ground  GND_supply   GND   0 6 0,
 11   3_8milsquare  -2025.1  -697.2   0 signal_digital cmos_io_pad  B2[2] 2 3 2,
 12   3_8milsquare  -2025.1  -914.9   0 signal_digital cmos_io_pad  B2[3] 2 3 3,
 13   3_8milwide    -2025.1 -1241.6   0 supply_power   VCC_supply   VCC   0 5 0,
 14   3_8milsquare  -2025.1 -1581.7   0 signal_digital cmos_io_pad  B2[4] 2 3 4,
 15   3_8milsquare  -1891.5 -1976.4   0 signal_digital cmos_io_pad  B2[5] 2 3 5,
 16   3_8milsquare  -1618.7 -1976.4   0 supply_ground  GND_supply   GND   0 6 0,
 17   3_8milsquare  -1361.2 -1976.4   0 signal_digital cmos_io_pad  B2[6] 2 3 6,
 18   3_8milsquare  -1040.9 -1976.4   0 signal_digital cmos_io_pad  B2[7] 2 3 7,
 19   3_8milsquare  -774.7 -1976.4   0 signal_digital cmos_input_pad DIR2 2 2 0,
 20   3_8milsquare   -506.5 -1976.4   0 signal_digital cmos_io_pad  B2[8] 2 3 8,
 21   3_8milsquare   -217.9 -1976.4   0 signal_digital cmos_output_pad TDO, | .....
```


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Suggested Improvements in IBIS

- **Need well defined measurement methodology for ALL parameters. Diagram of example setup and equipment. How is [RAMP] measured? [CLAMP] voltage range is high enough to require specialized digital curve tracer it appears.**
- **Process derating (temperature, supply voltage and process %) is not explicit. Example extremes apply to CMOS but not all other extremes technologies. Should at least state what extreme conditions were used even if databook values.**
- **Voltage reference to power supply in [pull_up] is counter intuitive and does not have the advantage of "tracking" with the supply voltage as intended.**
- **Add 3-D (I/V/t) modeling to [pull_up] and [pull_down] (BIRD issue).**
- **Do the range assumptions for 2*Vcc, -Vcc, etc. apply for 3v parts?**
- **Improve the package circuit model so beam lead (TAB, ribbon) lead devices can be incorporated nicely.**
- **Clean up and normalize syntax. Possibly change to SGML style for future considerations without requiring SGML DTD (LMC can help here).**

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