Asian IBIS Summit 2024 in Shanghai, PR China Minutes

Meeting Date: **October 25, 2024**

Meeting Location: **Shanghai, PR China**

VOTING MEMBERS AND 2024 PARTICIPANTS

Altair	(JuneSang Lee)
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Applied Simulation Technology	(Fred Balistreri)
Aurora System	(Dian Yang), Raj Raghuram, Haiwen Zhang*, Zelin Zuo*, Zhenguo Sun*, Zhen Guo*
Broadcom	(Yunong Gan)
Cadence Design Systems	Kyle Lake, Ambrish Varma, Jared James, John Phillips, Kristoffer Skytte, Baolong Li, Zuli Qin*, Jianpin Kong*, Shengli Wang*, Haojie Wang*, Yang Hou*
Celestica	(Sophia Feng)
Cisco Systems	(Stephen Scearce), Hong-Man Wu
Dassault Systemes	Stefan Paret, David Duque
GE Healthcare Technologies	(Balaji Sankarshanan)
Google	(Hanfeng Wang)
Huawei Technologies	Hang (Paul) Yan*
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Instituto de Telecomunicações	(Abdelgader Abdalla)
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Waymo	(Feng Wang), [Ji Zhang]
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Zuken	(Ralf Brüning), Markus Bücker
Zuken China	Tohishiro Hoshi*, Sheng Xu*, Lei Zhao*
Zuken USA	Lance Wang*

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Alps Alpine Co., Ltd.	Yasuaki Matoba
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Toyobo Co.	Saki Kawano
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Yamaha Corporation	Hiroyuki Kai
Zhejiang University	Ling Zhang
Zhejiang Uniview Technologies Co., Ltd.	Yifan Zhu*, Pin Jiang*, Shu Wang*

In the list above, attendees present at the meeting are indicated by "*" Those submitting an email ballot for their member organization for a scheduled vote are indicated by "^." Principal members or other

active members who have not attended are in parentheses “( ).” Participants who no longer are in the organization are in square brackets “[ ].”

UPCOMING MEETINGS

The connection information for future IBIS teleconferences is as follows:

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All teleconference meetings are 8:00 a.m. to 9:55 a.m. US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting.

NOTE: "AR" = Action Required.

SUMMIT MINUTES - SUMMARY AND LINKS

The 2024 IBIS Summit at Shanghai, PR China was held October 25, 2024 as an in-person-only conference. In attendance, there were approximately 44 individuals representing 15 companies, including representatives from 10 IBIS member organizations.

The following minutes capture the agenda and summarize presentations. A recording is currently available with time indices below, also copies of each presentation if available are accessible at this link:

Link: https://ibis.org/summits/oct24b/

09:00 **SIGN IN**

- Vendor Tables Open at 9:00

09:30 **MEETING WELCOME**
(Start 00:00:00, To 00:05:15, recording 1)

Wang, Lance (Chair, IBIS Open Forum)
(Zuken, USA)

Lance Wang announced the Asian IBIS Summit 2024 in Shanghai, PR China had officially started. He welcomed attendees and thanked all the sponsors of this event as follows:

- Ansys
- Empyrean
- Aurora System
- Cadence Design Systems

Lance expressed thanks for their generous support for this IBIS Summit meeting.

09:40 **IBIS Chair's Report**
(Start 00:05:45, To 00:29:45)

Wang, Lance (Zuken, USA)

Lance Wang introduced himself as the Chair of the IBIS Open Forum. Lance presented on the following:

IBIS has 28 members currently and presented a chart of annual membership since 1995. A chart was provided showing membership on an annual basis, where the increase and decrease of membership had been due to acquisitions of companies by other companies or startups of new product companies. There has been some discussion to add membership to include rate tiers with a special rate for smaller companies.

Lance presented on the following:

- 28 IBIS Members
  - 2 new members.
- Roster of IBIS Officers June 2024 – May 2025
  - Summary of elected individuals representing organizations on board
- IBIS Meetings (weekly teleconferences)
- IBIS Open Forum teleconference every 3 weeks (Fridays, 08:00 PT)
- IBIS Summit meetings (USA and international)
  - DesignCon, IEEE SPI, IEEE EMC+SIPI, Shanghai, Tokyo (JEITA-organized)
- Participants: ~290 in 2023 (~280 in 2022)
- SAE Industry Technologies Consortia is the parent organization of the IBIS Open Forum
  - SAE ITC provides financial, legal, and other services to the IBIS Open Forum
  - SAE ITC representatives: Tammy Patton, Phyllis Gross, and Rich Demary
  - Link: https://www.sae-itc.com/
- Task Groups
  - Typically meet on weekly basis
  - Advanced Technology Modeling (ATM) task group
    - Chair: Arpad Muranyi, Siemens EDA
    - https://ibis.org/atm_wip/
    - Develop non-interconnect technical BIRDs
  - Editorial task group
    - Chair: Michael Mirmak, Intel

        - https://ibis.org/editorial_wip/
        - Produce IBIS specification documents
    - Interconnect task group
        - Chair: Michael Mirmak, Intel
        - https://ibis.org/interconn_wip/
        - Develop on-die/package/module/connector interconnect modeling BIRDs
    - Quality task group
        - Acting Chair: Randy Wolff, Siemens EDA
        - https://ibis.org/quality_wip/
        - Oversee IBISCHK parser testing and development
- IBIS Milestones
    - Various accomplishments and industry-associated activities
- Planning for IBIS Version 8.0
    - Listing of BIRD IDs officially considered for IBIS 8.0 specification content
- BIRD description (Buffer Issue Resolution Document)
    - Summary of present BIRDs considered for adoption
- TSIRD description (Touchstone Issue Resolution Document)
    - Summary of present TSIRDs considered for adoption
- IBISCHK Development
    - IBISCHK Parser Issue Reports (BUGs)
    - Summary of present BUGs considered for resolution
- TSCHK Development
    - TSCHK Parser Issue Reports (BUGs)
    - Summary of present BUGs considered for resolution
    - How to submit bug reports for IBISCHK and TSCHK/TSCHK2
- Recent and Future Developments in IBIS
    - Expanded system-level perspective
    - Power Integrity focused modeling
    - Multi-level analog buffer modeling
    - Interconnect modeling
    - Quality and Testing
    - Specification Clarification
- Invitation to participate in IBIS Open Forum and Task Groups:
    - “What else should we be looking at? Bring your ideas!”
    - Success of IBIS and Touchstone depends on active participation and volunteering
    - Task groups for technical discussion and document editing
    - IBIS email reflectors

    - Open Forum teleconferences for event planning and voting
    - Summit presentations
    - IBIS Board and task group volunteering
    - Writing BIRDs – Buffer Issue Resolution Documents
        - Official method for submitting proposed change to IBIS specification
        - Many developed collaboratively in task groups
        - Discussed and voted on in Open Forum meetings
- IBIS Website Resources
    - IBIS Summits
    - Task Group information
    - Member FAQ
    - Specification documents
    - BIRDs / ISSIRDs / TSIRDs
    - Email support
    - Syntax Parser Downloads
    - Link: https://www.ibis.org

(conclusion of IBIS Chair's Report)

Lance concluded the IBIS Chair's Report and asked for any questions. No questions were asked.

10:00 **Priorities and Alternatives for Touchstone 3.0 Port Mapping – Updated**
(Start 00:30:15, To 01:01:00)

Mirmak, Michael (Intel, USA) (recorded)

- Problem Statement
    - Given a set of S-parameters that describe a component, is there sufficient data
    - Current Touchstone 1.0 and 2.0 does not describe some component types
    - What is the relationship between ports (input vs. output)
    - What is the context of this device and how to use it?
- Multiple Proposals for Port Mapping
    - IBIS Interconnect Task Group is considering multiple options
    - Examples of both proposals thus far are included in the presented slides
    - Detailed information at link: https://ibis.org/interconnect_wip
- Proposed Requirements
    - Define unambiguous connections for simulation
    - Identify Port locations (e.g. X-Y location on a Layer of PCB)
    - Support automated creation of schematic symbols, test probe locations
    - Support generation and verification
    - Support IEEE 370 data quality features
    - Identify data status (Measured vs. Simulated)
    - Support swathing

    - Support addition of user-defined parameters
- “HL” Proposal Syntax Examples (Proposal 1 of 2 shown)
- “Y” Proposal Syntax Examples (Proposal 2 of 2 shown)
- Your Input is Needed!
    - Michael invited attendees and any interested members to contribute to this ongoing discussion in the IBIS Interconnect Task Group.
- Q+A session
    - Note: See recording for detailed slides and Q+A discussion.

A question was asked whether the Port Map all keyword/sub keyword/parameters must be presented, Lance Wang answered some are the optional keywords.

Copy of presentation for review at link: https://ibis.org/summits/oct24b/

10:30 **BREAK (20 minutes)**

- Refreshments and Vendor Tables
- Reconvene at 10:50

10:50 **Pole-Residue Data Format for Touchstone**
(Start 01:27:00, To 01:51:15)

Muranyi, Arpad (Siemens, USA)

- Background and Motivation
    - The size of Touchstone files has increased dramatically in recent years
        - This is due to models with more ports and more frequency points
    - Consequently, file size reduction is becoming an important need
    - The Pole-Residue format would serve this purpose very well
        - Fitted poles or similar techniques have been used by EDA vendors for decades
    - We just need a tool independent standardized syntax
        - The IBIS Open Forum decided to enhance Touchstone 3.0 with a Pole-Residue format
        - Goals and plans were discussed in a presentation at the SPI 2022 IBIS summit https://www.ibis.org/summits/may22/muranyi.pdf
    - TSIRD 7 was submitted to the IBIS Open Forum on February 14, 2024
        - After receiving some review comments, TSIRD 7.1 was submitted on May 7, 2024, and
        - TSIRD 7.2 was submitted on June 3, 2024, and approved on August 23, 2024
- Arpad introduced few examples with keywords and formulas

No questions were asked.

Copy of presentation for review at link: https://ibis.org/summits/oct24b/

11:10 **LPDDR5(X) Challenge and Simulations**
(Start 01:51:30, To 02:09:45)

Zhang, Haiwen (Aurora-System Inc) (Presenter)
Wang, Mengying (LCFC)

- LPDDR trend was introduced
- Pointed out the pain points for DDR5 and LPDDR5 designs
- Given out the solutions for trace, via and via stub in PCB designs
- Showed the simulation results for verifications

A Question was asked about how to read the simulation eye diagram results presented.

Copy of presentation for review at link: https://ibis.org/summits/oct24b/

11:35 **DDR IBIS-AMI Non-Linear Effect Modeling in Statistical Simulations**
(Start 02:10:15, To 02:27:30)

Ran, Xuefeng (Synopsys, PRC) (Presenter)
Yao, Chang (Synopsys, PRC)
Li, Kevin (Synopsys, PRC)
Zhou, Jianguo (Synopsys, PRC)

- Motivation
  - LTI (Linear Time-Invariant) model is used in statistical simulation
  - Disadvantages in LTI model
    - LTI model typically does not include non-linear gain compression effect
    - LTI model is less accurate comparing with NLTV models
  - Aim to include gain compression effect in LTI model, make it as close to NLTV (Non Linear Time-Variant) model as possible
- Proposed DDR5 IBIS-AMI Modeling Methodologies
  - Testbench topology
  - Parameter set-up follow these conditions
- Summary
  - Model gain compression effect in LTI model correctly
  - Statistical (LTI) simulation results can correlate well with both SPICE circuit simulations and bit-by-bit (NLTV) results

A question was asked if the presenter's TX model needs to be modified for this case. The answer in reply was no. Another question is how to read the comparison in slide 9.

Copy of presentation for review at link: https://ibis.org/summits/oct24b/

12:00 **NO COST LUNCHEON (90 minutes, hosted by sponsors)**

- Reconvene at 13:30
- Vendor Tables

13:30 **Modeling and Simulation of High Speed Serial Link Systems**
(Start 00:01:30, To 00:23:00, recording 2)

Zheng, Ming (ZTE, PRC)

- Problem Statement
  - Problems occur during the channel evaluation when the electrical interfaces rate reach 112Gbps:
    - It is difficult to filter out failed channels, based on passive channel specifications like ICN, FOM_ILD and ERL
    - Channel Operating Margin, a channel compliance evaluation method
      - Based on certain prerequisites, there may be some difference from the actual situation
    - Models from IP vendors
      - In some instances, simulation may prove to be time-consuming
      - Simulation results are supposed to be calibrated according to test results and test environment
- Conclusion
  - The challenges arise when designing a system channel and evaluating its end-to-end performance, as we described in “Problem Statement” part. This method is performed on LR channels of an orthogonal system in a real-world application, the results indicate that it has quite good performance both in terms of simulation time and precision.
  - Two tips for faster simulation:
    - Preset Tx FIR and CTLE config according to channel loss
    - Proposal for a more efficient way to perform MLSE
  - Using the aforementioned method, we are capable of capturing the enhancement in MLSE performance over DFE and predicting BER, all while preserving a reasonable simulation duration.

No questions were asked.

Copy of presentation for review at link: https://ibis.org/summits/oct24b/

13:55 **Chiplet Signal Integrity Simulation**
(Start 00:24:30, To 00:46:15)

Jiang, Xiuguo (Keysight Technologies, PRC)
Li, Chaun-Bao (Keysight Technologies, PRC)

- What is Chiplet
  - A chiplet is an IC designed to be combined with other chiplets in a single package
  - System on a single package rather than System on a Chip (SoC)
    - Avoiding one gigantic monolithic die by dividing it into several smaller dies and integrating them into a single package
    - Cost-effectiveness, power efficiency (lower picojoule/bit), improved thermal performance, higher yield, and faster development times
    - Similar to conventional SiP, SoP, PoP, PiP, etc., but with much higher-level integration based on advanced packaging technologies such as 3DIC and heterogeneous integration
  - Multi-technology integration encompassing high-speed computing, RF, optics, etc.

    - Foundry-driven integration and standardization activities, such as TSMC 3DFabric and 3DBlox, are significantly shaping the landscape
    - Wide reaching applications across various markets
        - Data centers and cloud computing
        - Telecommunications and networking
        - High performance computing (HPC)
        - Aerospace and defense
        - And more…
- Summary of Chiplet Simulation
    - It is very important to analyze chiplets from D2D to D2D at a system level using smart design environment, it can help engineers find and solve problems as quickly as possible
    - Need to support:
        - differential forwarded clock in UCIe, BoW, AIB standard.
        - Standard Driven VTF Measurements

No questions were asked.

Copy of presentation for review at link: https://ibis.org/summits/oct24b/

14:25 **The Optimization of IBIS-AMI Model Parameters with Machine Learning Algorithms**
(Start 00:47:15, To 01:08:30)

Kong, Jianping (Cadence Design Systems, PRC)

- Machine Learning for Optimization
    - Machine Learning:
        - The use and development of computer systems that can learn and adapt without following explicit instructions, by using algorithms and statistical models to analyze and draw inferences from patterns in data
    - Optimization:
        - An act, process, or methodology of making something (such as a design, system, or decision) as fully perfect, functional, or effective as possible
    - Goal: Apply a machine learning optimization algorithm that will optimize the equalization parameters to maximize/minimize an output from the simulation results
    - These classes of ML algorithms are useful when the objective function is computationally expensive or time-consuming to evaluate
- Conclusions:
    - A machine learning algorithm was applied to the optimization of AMI parameters in a serial link simulation
    - The results show that the algorithm was able to find good results for three different channels, indicating the robustness of the algorithm
    - This method was able to find a good set of parameters in fewer simulations than if an exhaustive method had been deployed, saving the use of limited compute resources
    - In most test cases, it was found that only 100 simulations were needed to find the best set of parameters. Compare this to the over 7 million simulations for an exhaustive search

A question was asked this needs about 100 test cases to train as mentioned. It seems a bit high than expected. Answer was that 100 is the maximum cases number we set. In the real cases, it might only need 60-70 test cases.

Copy of presentation for review at link: https://ibis.org/summits/oct24b/

14:55 **CONCLUDING ITEMS**
(Start 01:08:45, To 01:12:45)

Lance Wang thanked the sponsors again for making this meeting possible:

- Ansys
- Empyrean
- Aurora System
- Cadence Design Systems

Lance announced the conclusion of the Asian IBIS Summit 2024 in Shanghai, PR China.

15:00 **END OF IBIS SUMMIT MEETING**

- The IBIS summit meeting concluded.

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NOTES

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  - https://www.freelists.org/list/ibis-users
- To subscribe to or unsubscribe from one of the Task Group email lists: ibis-macro@freelists.org, ibis-interconn@freelists.org, ibis-editorial@freelists.org, or ibis-quality@freelists.org:
  - https://www.freelists.org/list/ibis-macro
  - https://www.freelists.org/list/ibis-interconn
  - https://www.freelists.org/list/ibis-editorial
  - https://www.freelists.org/list/ibis-quality
- To inquire about joining the IBIS Open Forum as a voting Member.
- To purchase a license for the IBIS parser source code.
- To report bugs or request enhancements to the free software tools: ibischk7, tschk2, icmchk1, s2IBIS, s2IBIS2 and s2iplt.

The BUG Report Form for ibischk resides along with reported BUGs at:

https://ibis.org/bugs/ibischk/
https://ibis.org/ bugs/ibischk/bugform.txt

The BUG Report Form for tschk2 resides along with reported BUGs at:

https://ibis.org/bugs/tschk/
https://ibis.org/bugs/tschk/bugform.txt

The BUG Report Form for icmchk resides along with reported BUGs at:

https://ibis.org/bugs/icmchk/
https://ibis.org/bugs/icmchk/icm_bugform.txt

To report s2IBIS, s2IBIS2 and s2iplt bugs, use the Bug Report Forms which reside at:

https://ibis.org/bugs/s2IBIS/bugs2i.txt
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Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

https://ibis.org/

Check the IBIS file directory on IBIS.org for more information on previous discussions and results:

https://ibis.org/directory.html

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SAE STANDARDS BALLOT VOTING STATUS (attendee X; absent -)

Organization	Interest Category	Standards Ballot Voting Status	Sept 13, 2024	Oct 4, 2024	Oct 22, 2024	Oct 24, 2024
Altair	User	Inactive	-	-	-	-
AMD (Xilinx)	Producer	Inactive	-	-	X	-
Analog Devices	Producer	Inactive	-	-	-	-
Ansys	User	Active	X	X	X	X
Applied Simulation Technology	User	Inactive	-	-	-	-
Aurora System	User	Active	-	-	X	X
Broadcom Ltd.	Producer	Inactive	-	-	-	-
Cadence Design Systems	User	Active	X	X	X	X
Celestica	User	Inactive	-	-	-	X
Cisco Systems	User	Inactive	-	-	-	-
Dassault Systems	User	Inactive	-	-	-	-
GE Healthcare Technologies	User	Inactive	-	-	-	-
Google	User	Inactive	-	-	-	-
Huawei Technologies	Producer	Inactive	-	-	-	X
Infineon Technologies AG	Producer	Inactive	-	-	-	-
Intel Corp.	Producer	Active	X	X	-	X
Keysight Technologies	User	Active	-	-	X	X
Marvell	Producer	Inactive	-	-	-	-
MathWorks	User	Inactive	X	X	-	-
Micron Technology	Producer	Inactive	-	-	X	-
MST EMC Lab	User	Inactive	-	-	-	-
SI-Clarity	User	Inactive	X	X	-	-
Siemens EDA	User	Active	X	X	X	-
STMicroelectronics	Producer	Inactive	-	-	-	-
Synopsys	User	Active	X	X	X	X
ZTE Corp.	User	Inactive	-	-	-	X
Zuken	User	Active	X	X	X	X

= Temporarily not a voting member

Criteria for SAE member in good standing:

- Must attend two consecutive meetings to establish voting membership.
- Membership dues current
- Must not miss two consecutive meetings (voting by email counts as attendance)

Interest categories associated with SAE standards ballot voting are:

- Users - members that utilize electronic equipment to provide services to an end user.
- Producers - members that supply electronic equipment.

General Interest - members are neither producers nor users. This category includes, but is not limited to, government, regulatory agencies (state and federal), researchers, other organizations, and associations, and/or consumers.