Version 0.1

Information Model Of

I/O Buffer Specification

(IBIS) Version 2.0

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Version 0.1 Information Model Of I/O Buffer Specification (IBIS) Version 2.0

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1.0 Introduction

This document contains an information model of the I/O Buffer Specification (IBIS) Version 2.0. Its contents have not been reviewed by any competent authority.

2.0 Component UoF

```
1       SCHEMA component_uof;
2
3       REFERENCE FROM file_uof (ibis_file);
4
5       REFERENCE FROM package_model_uof (package_model);
6
7       REFERENCE FROM pin_model_uof (pin_model);
8
9       REFERENCE FROM signal_uof (signal);
10
11      REFERENCE FROM support_uof (capacitance_range,
12                                  capacitance_value,
13                                  inductance_range,
14                                  inductance_value,
15                                  resistance_range,
16                                  resistance_value,
17                                  time_range,
18                                  voltage_value);
19
20      (*
21      ------------------------------------------------------------------
22      *)
23
24      ENTITY bus;
25        bus_name                    : STRING (15);
26      DERIVE
27        connects                    : SET OF pin_map :=
28                            pulls_down + pulls_up + clamps_to_ground + clamps_to_power;
29      INVERSE
30        pulls_down                  : SET OF pin_map FOR pulldown_reference;
31        pulls_up                    : SET OF pin_map FOR pullup_reference;
32        clamps_to_ground            : SET OF pin_map FOR ground_clamp;
33        clamps_to_power             : SET OF pin_map FOR power_clamp;
34      WHERE
35        at_least_one_connected_pin_is_power_or_ground :
36          QUERY (c <* connects |
37                 ['COMPONENT_UOF.GROUND_PIN',
38                  'COMPONENT_UOF.POWER_PIN'] * TYPEOF (c))
39          <> [];
40        the_bus_cannot_connect_unconnected_pins :
41          QUERY (c <* connects |
42                 'COMPONENT_UOF.NOT_CONNECTED_PIN' IN TYPEOF (c)) = [];
43      END_ENTITY;
44
45      (*
46      ------------------------------------------------------------------
47      *)
48
49      ENTITY component;
50        component_name              : STRING (40);
51        manufacturer_name           : STRING (40);
52        default_resistance_range    : resistance_range;
53        default_inductance_range    : inductance_range;
54        default_capacitance_range   : capacitance_range;
55        has_pins                    : SET [1 : ?] OF pin;
56        uses_package_model          : OPTIONAL package_model;
57        has_pin_mapping             : OPTIONAL pin_mapping;
58        has_pin_differentials       : OPTIONAL SET [1 : ?] OF pin_differential;
59      INVERSE
60        containing_file             : ibis_file FOR components;
61      END_ENTITY;
62
63      (*
64      ------------------------------------------------------------------
65      *)
66
67      ENTITY defined_pin
68          SUBTYPE OF (pin);
```

```
69        conforms_to                : pin_model;
70      END_ENTITY;
71
72      (*
73      -------------------------------------------------------------------
74      *)
75
76      ENTITY ground_pin
77          SUBTYPE OF (predefined_pin);
78      END_ENTITY;
79
80      (*
81      -------------------------------------------------------------------
82      *)
83
84      ENTITY not_connected_pin
85          SUBTYPE OF (predefined_pin);
86      END_ENTITY;
87
88      (*
89      -------------------------------------------------------------------
90      *)
91
92      ENTITY pin
93          ABSTRACT SUPERTYPE OF (ONEOF (predefined_pin,
94                                        defined_pin));
95        pin_name                   : STRING (5);
96        has_signal                 : signal;
97        override_resistance        : OPTIONAL resistance_value;
98        override_inductance        : OPTIONAL inductance_value;
99        override_capacitance       : OPTIONAL capacitance_value;
100     INVERSE
101       component                  : component FOR has_pins;
102     END_ENTITY;
103
104     (*
105     -------------------------------------------------------------------
106     *)
107
108     ENTITY pin_differential;
109       non_inverting_pin          : pin;
110       inverting_pin              : pin;
111       voltage_differential       : voltage_value;
112       delay                      : time_range;
113     INVERSE
114       component                  : component FOR has_pin_differentials;
115     WHERE
116       the_non_inverting_pin_is_in_the_component :
117         non_inverting_pin IN component.has_pins;
118       the_inverting_pin_is_in_the_component :
119         inverting_pin IN component.has_pins;
120     END_ENTITY;
121
122     (*
123     -------------------------------------------------------------------
124     *)
125
126     ENTITY pin_map;
127       for_pin                    : pin;
128       pulldown_reference         : OPTIONAL bus;
129       pullup_reference           : OPTIONAL bus;
130       ground_clamp               : OPTIONAL bus;
131       power_clamp                : OPTIONAL bus;
132     INVERSE
133       mapping                    : pin_mapping FOR members;
134     UNIQUE
135       one_map_per_pin :
136         for_pin;
137     WHERE
138       the_pin_is_a_pin_of_the_component :
```

```
139         for_pin IN mapping.component.has_pins;
140     END_ENTITY;
141
142     (*
143     -------------------------------------------------------------------------
144     *)
145
146     ENTITY pin_mapping;
147       members                     : SET [1 : ?] OF pin_map;
148     INVERSE
149       component                   : component FOR has_pin_mapping;
150     WHERE
151       there_is_a_pin_map_for_each_pin :
152         SIZEOF (members) = SIZEOF (component.has_pins);
153     END_ENTITY;
154
155     (*
156     -------------------------------------------------------------------------
157     *)
158
159     ENTITY power_pin
160         SUBTYPE OF (predefined_pin);
161     END_ENTITY;
162
163     (*
164     -------------------------------------------------------------------------
165     *)
166
167     ENTITY predefined_pin
168         ABSTRACT SUPERTYPE OF (ONEOF (power_pin,
169                                       ground_pin,
170                                       not_connected_pin))
171         SUBTYPE OF (pin);
172     END_ENTITY;
173
174     END_SCHEMA;
175
```

3.0 File UoF

```
176   SCHEMA file_uof;
177
178   REFERENCE FROM component_uof (component);
179
180   (*
181   ------------------------------------------------------------------
182   *)
183
184   TYPE
185     file_status      = ENUMERATION OF (silicon_and_file_in_development,
186                                        pre_silicon_file_from_silicon_model_only,
187                                        file_correlated_to_silicon_measurements,
188                                        mature_product);
189   END_TYPE;
190
191   (*
192   ------------------------------------------------------------------
193   *)
194
195   ENTITY ibis_file;
196     file_name                   : STRING (8);
197     status                      : file_status;
198     revision                    : INTEGER;
199     date                        : OPTIONAL STRING;
200     source                      : OPTIONAL STRING;
201     notes                       : OPTIONAL STRING;
202     disclaimer                  : OPTIONAL STRING;
203     components                  : SET [1 : ?] OF component;
204   WHERE
205     the_revision_is_non_negative :
206       revision >= 0;
207   END_ENTITY;
208
209   END_SCHEMA;
210
```

4.0 Package Model UoF

```
211   SCHEMA package_model_uof;
212
213   REFERENCE FROM support_uof (capacitance_value,
214                               inductance_value,
215                               positive_integer_value,
216                               resistance_value);
217
218   (*
219   ------------------------------------------------------------------------
220   *)
221
222   ENTITY package_model;
223     model_name                  : STRING (40);
224     part_manufacturer_name      : STRING (40);
225     package_manufacturer_name   : STRING (40);
226     description                 : STRING (60);
227     number_of_pins              : positive_integer_value;
228     package_pins                : LIST [number_of_pins : number_of_pins]
229                                   OF package_pin;
230     resistance_matrix           : SET [matrix_size : matrix_size]
231                                   OF pin_to_pin_resistance;
232     capacitance_matrix          : SET [matrix_size : matrix_size]
233                                   OF pin_to_pin_capacitance;
234     inductance_matrix           : SET [matrix_size : matrix_size]
235                                   OF pin_to_pin_inductance;
236   DERIVE
237     matrix_size                 : positive_integer_value :=
238                                   number_of_pins * (number_of_pins + 1) / 2;
239   END_ENTITY;
240
241   (*
242   ------------------------------------------------------------------------
243   *)
244
245   ENTITY package_pin;
246     pin_name                    : STRING (5);
247   INVERSE
248     package                     : package_model FOR package_pins;
249   END_ENTITY;
250
251   (*
252   ------------------------------------------------------------------------
253   *)
254
255   ENTITY pin_to_pin_capacitance;
256     between_pins                : SET [2 : 2] OF package_pin;
257     has_capacitance             : capacitance_value;
258   INVERSE
259     package                     : package_model FOR capacitance_matrix;
260   UNIQUE
261     only_one_capacitance_value_per_pin_set :
262       between_pins;
263   WHERE
264     each_pin_is_a_pin_of_the_package :
265       QUERY (p <* between_pins | p.package :=: package) = between_pins;
266   END_ENTITY;
267
268   (*
269   ------------------------------------------------------------------------
270   *)
271
272   ENTITY pin_to_pin_inductance;
273     between_pins                : SET [2 : 2] OF package_pin;
274     has_inductance              : inductance_value;
275   INVERSE
276     package                     : package_model FOR inductance_matrix;
277   UNIQUE
278     only_one_inductance_value_per_pin_set :
```

```
279         between_pins;
280     WHERE
281       each_pin_is_a_pin_of_the_package :
282         QUERY (p <* between_pins | p.package :=: package) = between_pins;
283     END_ENTITY;
284
285     (*
286     ------------------------------------------------------------------------
287     *)
288
289     ENTITY pin_to_pin_resistance;
290       between_pins                : SET [2 : 2] OF package_pin;
291       has_resistance              : resistance_value;
292     INVERSE
293       package                     : package_model FOR resistance_matrix;
294     UNIQUE
295       only_one_resistance_value_per_pin_set :
296         between_pins;
297     WHERE
298       each_pin_is_a_pin_of_the_package :
299         QUERY (p <* between_pins | p.package :=: package) = between_pins;
300     END_ENTITY;
301
302     END_SCHEMA;
303
```

5.0 Pin Model UoF

```
304    SCHEMA pin_model_uof;
305
306    REFERENCE FROM signal_uof (signal);
307
308    REFERENCE FROM support_uof (capacitance_range,
309                                capacitance_value,
310                                not_yet_defined,
311                                ramp,
312                                resistance_range,
313                                resistance_value,
314                                temperature_range,
315                                voltage_current_table,
316                                voltage_range,
317                                voltage_value,
318                                waveform);
319
320    (*
321    ------------------------------------------------------------------------
322    *)
323
324    ENTITY ac_terminator_pin_model
325        SUBTYPE OF (terminator_pin_model);
326      SELF\terminator_pin_model.AC_resistance : resistance_range;
327      SELF\terminator_pin_model.AC_capacitance : capacitance_range;
328    END_ENTITY;
329
330    (*
331    ------------------------------------------------------------------------
332    *)
333
334    TYPE
335      enable                      = ENUMERATION OF (active_high,
336                                                    active_low);
337    END_TYPE;
338
339    (*
340    ------------------------------------------------------------------------
341    *)
342
343    ENTITY input_ecl_pin_model
344        SUBTYPE OF (pin_model);
345      SELF\pin_model.Vinl         : voltage_value;
346      SELF\pin_model.Vinh         : voltage_value;
347    END_ENTITY;
348
349    (*
350    ------------------------------------------------------------------------
351    *)
352
353    ENTITY input_output_ecl_pin_model
354        SUBTYPE OF (pin_model);
355      SELF\pin_model.Vinl         : voltage_value;
356      SELF\pin_model.Vinh         : voltage_value;
357      SELF\pin_model.has_ramp     : ramp;
358    END_ENTITY;
359
360    (*
361    ------------------------------------------------------------------------
362    *)
363
364    ENTITY input_output_open_drain_pin_model
365        SUBTYPE OF (pin_model);
366      SELF\pin_model.Vinl         : voltage_value;
367      SELF\pin_model.Vinh         : voltage_value;
368      SELF\pin_model.has_ramp     : ramp;
369    END_ENTITY;
370
371    (*
```

```
372     ------------------------------------------------------------------------
373     *)
374
375     ENTITY input_output_open_sink_pin_model
376         SUBTYPE OF (pin_model);
377       SELF\pin_model.Vinl         : voltage_value;
378       SELF\pin_model.Vinh         : voltage_value;
379       SELF\pin_model.has_ramp     : ramp;
380     END_ENTITY;
381
382     (*
383     ------------------------------------------------------------------------
384     *)
385
386     ENTITY input_output_open_source_pin_model
387         SUBTYPE OF (pin_model);
388       SELF\pin_model.Vinl         : voltage_value;
389       SELF\pin_model.Vinh         : voltage_value;
390       SELF\pin_model.has_ramp     : ramp;
391     END_ENTITY;
392
393     (*
394     ------------------------------------------------------------------------
395     *)
396
397     ENTITY input_output_pin_model
398         SUBTYPE OF (pin_model);
399       SELF\pin_model.Vinl         : voltage_value;
400       SELF\pin_model.Vinh         : voltage_value;
401       SELF\pin_model.has_ramp     : ramp;
402     END_ENTITY;
403
404     (*
405     ------------------------------------------------------------------------
406     *)
407
408     ENTITY input_pin_model
409         SUBTYPE OF (pin_model);
410       SELF\pin_model.Vinl         : voltage_value;
411       SELF\pin_model.Vinh         : voltage_value;
412     END_ENTITY;
413
414     (*
415     ------------------------------------------------------------------------
416     *)
417
418     ENTITY open_drain_pin_model
419         SUBTYPE OF (pin_model);
420       SELF\pin_model.has_ramp     : ramp;
421     END_ENTITY;
422
423     (*
424     ------------------------------------------------------------------------
425     *)
426
427     ENTITY open_sink_pin_model
428         SUBTYPE OF (pin_model);
429       SELF\pin_model.has_ramp     : ramp;
430     END_ENTITY;
431
432     (*
433     ------------------------------------------------------------------------
434     *)
435
436     ENTITY open_source_pin_model
437         SUBTYPE OF (pin_model);
438       SELF\pin_model.has_ramp     : ramp;
439     END_ENTITY;
440
441     (*
```

```
442     ------------------------------------------------------------------------
443     *)
444
445     ENTITY output_ecl_pin_model
446         SUBTYPE OF (pin_model);
447       SELF\pin_model.has_ramp     : ramp;
448     END_ENTITY;
449
450     (*
451     ------------------------------------------------------------------------
452     *)
453
454     ENTITY output_pin_model
455         SUBTYPE OF (pin_model);
456       SELF\pin_model.has_ramp     : ramp;
457     END_ENTITY;
458
459     (*
460     ------------------------------------------------------------------------
461     *)
462
463     ENTITY pin_model
464         ABSTRACT SUPERTYPE OF (ONEOF (input_pin_model,
465                                       input_output_pin_model,
466                                       input_output_open_drain_pin_model,
467                                       input_output_open_sink_pin_model,
468                                       input_output_open_source_pin_model,
469                                       input_ecl_pin_model,
470                                       input_output_ecl_pin_model,
471                                       terminator_pin_model,
472                                       output_pin_model,
473                                       tri_state_pin_model,
474                                       open_sink_pin_model,
475                                       open_drain_pin_model,
476                                       open_source_pin_model,
477                                       output_ecl_pin_model));
478       model_name                  : STRING (20);
479       silicon_die_capacitance      : capacitance_range;
480       has_polarity                : OPTIONAL polarity;
481       has_enable                  : OPTIONAL enable;
482       Vinl                        : OPTIONAL voltage_value;
483       Vinh                        : OPTIONAL voltage_value;
484       Vmeasure                    : OPTIONAL voltage_value;
485       reference_capacitance        : capacitance_value;
486       reference_resistance         : resistance_value;
487       signals                     : OPTIONAL SET [1 : ?] OF signal;
488       operating_temperature       : temperature_range;
489       pullup_reference            : voltage_range;
490       pulldown_reference          : voltage_range;
491       power_clamp_reference       : voltage_range;
492       ground_clamp_reference       : voltage_range;
493       pulldown                    : OPTIONAL voltage_current_table;
494       pullup                      : OPTIONAL voltage_current_table;
495       ground_clamp                : OPTIONAL voltage_current_table;
496       power_clamp                 : OPTIONAL voltage_current_table;
497       has_ramp                    : OPTIONAL ramp;
498       rising_waveforms            : OPTIONAL SET [1 : ?] OF waveform;
499       falling_waveforms           : OPTIONAL SET [1 : ?] OF waveform;
500     END_ENTITY;
501
502     (*
503     ------------------------------------------------------------------------
504     *)
505
506     TYPE
507       polarity                    = ENUMERATION OF (non_inverting,
508                                                     inverting);
509     END_TYPE;
510
511     (*
```

```
512     ------------------------------------------------------------------------
513     *)
514
515     ENTITY terminator_pin_model
516         SUBTYPE OF (pin_model);
517       resistance_to_ground        : OPTIONAL resistance_range;
518       resistance_to_power         : OPTIONAL resistance_range;
519       AC_resistance               : OPTIONAL resistance_range;
520       AC_capacitance              : OPTIONAL capacitance_range;
521     END_ENTITY;
522
523     (*
524     ------------------------------------------------------------------------
525     *)
526
527     ENTITY tri_state_pin_model
528         SUBTYPE OF (pin_model);
529       SELF\pin_model.has_ramp     : ramp;
530     END_ENTITY;
531
532     END_SCHEMA;
533
```

6.0 Signal UoF

```
534     SCHEMA signal_uof;
535
536     (*
537     ------------------------------------------------------------------------
538     *)
539
540     ENTITY signal;
541       signal_name                : STRING (20);
542     END_ENTITY;
543
544     END_SCHEMA;
545
```

7.0 Support UoF

```
546   SCHEMA support_uof;
547
548   (*
549   ------------------------------------------------------------------------
550   *)
551
552   ENTITY capacitance_range;
553     typical_value               : capacitance_value;
554     minimum_value               : OPTIONAL capacitance_value;
555     maximum_value               : OPTIONAL capacitance_value;
556   END_ENTITY;
557
558   (*
559   ------------------------------------------------------------------------
560   *)
561
562   TYPE
563     capacitance_value           = non_negative_real;
564   END_TYPE;
565
566   (*
567   ------------------------------------------------------------------------
568   *)
569
570   ENTITY current_range;
571     typical_value               : current_value;
572     minimum_value               : OPTIONAL current_value;
573     maximum_value               : OPTIONAL current_value;
574   END_ENTITY;
575
576   (*
577   ------------------------------------------------------------------------
578   *)
579
580   TYPE
581     current_value               = REAL;
582   END_TYPE;
583
584   (*
585   ------------------------------------------------------------------------
586   *)
587
588   ENTITY inductance_range;
589     typical_value               : inductance_value;
590     minimum_value               : OPTIONAL inductance_value;
591     maximum_value               : OPTIONAL inductance_value;
592   END_ENTITY;
593
594   (*
595   ------------------------------------------------------------------------
596   *)
597
598   TYPE
599     inductance_value            = non_negative_real;
600   END_TYPE;
601
602   (*
603   ------------------------------------------------------------------------
604   *)
605
606   TYPE
607     positive_integer_value      = INTEGER;
608   WHERE
609     it_is_positive :
610       SELF > 0;
611   END_TYPE;
612
613   (*
```

```
614     ------------------------------------------------------------------------
615     *)
616
617     TYPE
618       non_negative_real           = REAL;
619     WHERE
620       it_is_non_negative :
621         SELF >= 0;
622     END_TYPE;
623
624     (*
625     ------------------------------------------------------------------------
626     *)
627
628     FUNCTION not_yet_defined : BOOLEAN;
629       RETURN (TRUE);
630     END_FUNCTION;
631
632     (*
633     ------------------------------------------------------------------------
634     *)
635
636     ENTITY ramp;
637       rise_ramp                   : voltage_rate_range;
638       fall_ramp                   : voltage_rate_range;
639       load_resistance             : resistance_value;
640     END_ENTITY;
641
642     (*
643     ------------------------------------------------------------------------
644     *)
645
646     ENTITY resistance_range;
647       typical_value               : resistance_value;
648       minimum_value               : OPTIONAL resistance_value;
649       maximum_value               : OPTIONAL resistance_value;
650     END_ENTITY;
651
652     (*
653     ------------------------------------------------------------------------
654     *)
655
656     TYPE
657       resistance_value            = non_negative_real;
658     END_TYPE;
659
660     (*
661     ------------------------------------------------------------------------
662     *)
663
664     ENTITY temperature_range;
665       typical_value               : temperature_value;
666       minimum_value               : OPTIONAL temperature_value;
667       maximum_value               : OPTIONAL temperature_value;
668     END_ENTITY;
669
670     (*
671     ------------------------------------------------------------------------
672     *)
673
674     TYPE
675       temperature_value           = REAL;
676     WHERE
677       it_is_above_absolute_zero :
678         SELF > -273.16;
679     END_TYPE;
680
681     (*
682     ------------------------------------------------------------------------
683     *)
```

```
684
685     ENTITY time_range;
686       typical_value               : time_value;
687       minimum_value               : OPTIONAL time_value;
688       maximum_value               : OPTIONAL time_value;
689     END_ENTITY;
690
691     (*
692     ------------------------------------------------------------------------
693     *)
694
695     TYPE
696       time_value                  = non_negative_real;
697     END_TYPE;
698
699     (*
700     ------------------------------------------------------------------------
701     *)
702
703     ENTITY voltage_current_map;
704       for_voltage                 : voltage_value;
705       current                     : current_range;
706     END_ENTITY;
707
708     (*
709     ------------------------------------------------------------------------
710     *)
711
712     ENTITY voltage_current_table;
713       members                     : LIST [2 : 100] OF voltage_current_map;
714     WHERE
715       the_table_is_monotonic :
716         not_yet_defined;
717     END_ENTITY;
718
719     (*
720     ------------------------------------------------------------------------
721     *)
722
723     ENTITY voltage_range;
724       typical_value               : voltage_value;
725       minimum_value               : OPTIONAL voltage_value;
726       maximum_value               : OPTIONAL voltage_value;
727     END_ENTITY;
728
729     (*
730     ------------------------------------------------------------------------
731     *)
732
733     ENTITY voltage_rate;
734       voltage_change              : voltage_value;
735       in_time                     : time_value;
736     END_ENTITY;
737
738     (*
739     ------------------------------------------------------------------------
740     *)
741
742     ENTITY voltage_rate_range;
743       typical_value               : voltage_rate;
744       minimum_value               : OPTIONAL voltage_rate;
745       maximum_value               : OPTIONAL voltage_rate;
746     END_ENTITY;
747
748     (*
749     ------------------------------------------------------------------------
750     *)
751
752     TYPE
753       voltage_value               = REAL;
```

```
754     END_TYPE;
755
756     (*
757     ------------------------------------------------------------------------
758     *)
759
760     ENTITY waveform;
761       fixture_resistance          : resistance_value;
762       fixture_voltage             : resistance_value;
763       fixture_capacitance         : capacitance_value;
764       fixture_inductance          : inductance_value;
765       dut_resistance              : resistance_value;
766       dut_inductance              : inductance_value;
767       dut_capacitance             : capacitance_value;
768       members                     : LIST [1 : 100] OF waveform_element;
769     WHERE
770       the_members_increase_in_time :
771         not_yet_defined;
772     END_ENTITY;
773
774     (*
775     ------------------------------------------------------------------------
776     *)
777
778     ENTITY waveform_element;
779       at_time                     : time_value;
780       voltage                     : voltage_range;
781     INVERSE
782       the_waveform                : waveform FOR members;
783     UNIQUE
784       the_time_is_unique_within_the_waveform :
785         at_time, the_waveform;
786     END_ENTITY;
787
788     END_SCHEMA;
```

8.0 Glossary

Within this section references to keywords and sub-parameters refer to objects defined within the I/O Buffer Information Specification (IBIS) Version 2.0.

8.1 ac_terminator_pin_model

An **ac_terminator_pin_model** is a **pin_model** of model type terminator. The subtype **ac_terminator_pin_model** has been specified as it is mentioned in the description of Rgnd etc.

See keyword [Model], sub-parameter Model_type.

8.2 bus

The description of **pin_mapping** implies the existence of a **bus**. Although mention is made of a power or ground **bus**, it is not clear if the entity **bus** should be sub-typed.

See keyword [Pin Mapping].

8.3 capacitance_range

A **capacitance_range** is a range of **capacitance_values**. Only the typical value is mandatory.

8.4 capacitance_value

A **capacitance_value** is a capacitance measured in Farads.

8.5 component

A **component** is a description of an integrated circuit.

See keyword [component].

8.6 current_range

A **current_range** is a range of **current_values**. Only the typical value is mandatory.

8.7 current_value

A **current_value** is a current measured in Amperes.

8.8 defined_pin

A **defined_pin** is a **pin** which is non-standard and therefore is described by a **pin_model**.

See keyword [Pin].

8.9 enable

An **enable** value specified whether a **pin** should be considered when the voltage is high or low.

See keyword [Model], sub-parameter Enable.

8.10 file_status

A **file_status** is the standard part of a file revision.

See keyword [File Rev].

8.11 ground_pin

A **ground_pin** is a **pin** which conforms to the standard model of GROUND.

See keyword [Pin].

8.12 ibis_file

An **ibis_file** is a description of the electronic behavior of integrated circuit input/output characteristics.

8.13 inductance_range

A **inductance_range** is a range of **inductance_values**. Only the typical value is mandatory.

8.14 inductance_value

An **inductance_value** is an inductance measured in Henries.

8.15 input_ecl_pin_model

An **input_ecl_pin_model** is a **pin_model** of model type Input ECL.

See keyword [Model], sub-parameter Model_type.

8.16 input_output_ecl_pin_model

An **input_output_ecl_pin_model** is a **pin_model** of model type I/O ECL.

See keyword [Model], sub-parameter Model_type.

8.17 input_output_open_drain_pin_model

An **input_output_open_drain_pin_model** is a **pin_model** of model type I/O_open_drain.

See keyword [Model], sub-parameter Model_type.

8.18 input_output_open_sink_pin_model

An **input_output_open_sink_pin_model** is a **pin_model** of model type I/O_open_sink.

See keyword [Model], sub-parameter Model_type.

8.19 input_output_open_source_pin_model

An **input_output_open_source_pin_model** is a **pin_model** of model type I/O_open_source.

See keyword [Model], sub-parameter Model_type.

8.20 input_output_pin_model

An **input_output_pin_model** is a **pin_model** of model type I/O.

See keyword [Model], sub-parameter Model_type.

8.21 input_pin_model

An **input_pin_model** is a **pin_model** of model type Input.

See keyword [Model], sub-parameter Model_type.

8.22 non_negative_real

A **non_negative_real** is a real value which is greater than or equal to zero.

8.23 not_connected_pin

A **not_connected_pin** is a **pin** which conforms to the standard model of NOT CONNECTED.

See keyword [Pin].

8.24 not_yet_defined

The **not_yet_defined** function is used within the model where the exact realization of a constraint within EXPRESS has not yet been determined.

8.25 open_drain_pin_model

An **open_drain_pin_model** is a **pin_model** of model type Open_drain.

See keyword [Model], sub-parameter Model_type.

8.26 open_sink_pin_model

An **open_sink_pin_model** is a **pin_model** of model type Open_sink.

See keyword [Model], sub-parameter Model_type.

8.27 open_source_pin_model

An **open_source_pin_model** is a **pin_model** of model type Open_source.

See keyword [Model], sub-parameter Model_type.

8.28 output_ecl_pin_model

An **output_ecl_pin_model** is a **pin_model** of model type Output_ECL.

See keyword [Model], sub-parameter Model_type.

8.29 output_pin_model

An **output_pin_model** is a **pin_model** of model type Output.

See keyword [Model], sub-parameter Model_type.

8.30 package_model

A **package_model** is a description of the analog behavior of a package.

See keyword [Define Package Model].

8.31 package_pin

A **package_pin** is a terminal of a **package_model**.

See keyword [Pin Numbers].

8.32 pin

A **pin** is an external pin of a **component**.

See keyword [Pin].

8.33 pin_differential

A **pin_differential** is the voltage differential and time delay between associated differential **pins**. The description suggests that a **pin** should be identified as a differential **pin**. However, it is not clear how such semantics should be modeled.

See keyword [Diff Pin].

8.34 pin_map

A **pin_map** is the association of a **pin** to power and ground **buss**.

See keyword [Pin Mapping].

8.35 pin_mapping

A **pin_mapping** is the association of **pins** to power and ground **buss**.

See keyword [Pin Mapping].

8.36 pin_model

A **pin_model** is a description of the electronic behavior of a **pin**.

See keyword [Model].

8.37 pin_to_pin_capacitance

A **pin_to_pin_capacitance** is the capacitance between two **package_pins**.

See keyword [Capacitance Matrix].

8.38 pin_to_pin_inductance

A **pin_to_pin_inductance** is the inductance between two **package_pins**.

See keyword [Capacitance Matrix].

8.39 pin_to_pin_resistance

A **pin_to_pin_resistance** is the resistance between two **package_pins**.

See keyword [Capacitance Matrix].

8.40 polarity

A **polarity** value specifies whether or not a **pin** inverts logic values.

See keyword [Model], sub-parameter Polarity.

8.41 positive_integer_value

A **positive_integer_value** is an integer value which is greater than zero.

8.42 power_pin

A **power_pin** is a **pin** which conforms to the standard model of POWER.

See keyword [Pin].

8.43 predefined_pin

A **predefined_pin** is a **pin** which conforms to the standard model.

See keyword [Pin].

8.44 ramp

A **ramp** is the rise and fall rates of a buffer for a specific load resistance.

See keyword [Ramp].

8.45 resistance_range

A **resistance_range** is a range of **resistance_values**. Only the typical value is mandatory.

8.46 resistance_value

A **resistance_value** is a resistance measured in Ohms.

8.47 signal

A **signal** is a flow of information which is carried via a **pin**.

See keyword [Pin], sub-parameter signal_name.

8.48 temperature_range

A **temperature_range** is a range of **temperature_values**. Only the typical value is mandatory.

8.49 temperature_value

A **temperature_value** is a temperature measured in degrees Celsius.

8.50 terminator_pin_model

A **terminator_pin_model** is a **pin_model** of model type Terminator.

See keyword [Model], sub-parameter Model_type.

8.51 time_range

A **time_range** is a range of **time_values**. Only the typical value is mandatory.

8.52 time_value

A **time_value** is a time measured in Seconds.

8.53 tri_state_pin_model

A **tri_state_pin_model** is a **pin_model** of model type 3-State.

See keyword [Model], sub-parameter Model_type.

8.54 voltage_current_map

A **voltage_current_map** specifies the range of current used by a **pin** for a given **voltage_value**.

8.55 voltage_current_table

A **voltage_current_table** specifies the **current_ranges** used by a **pin** for the specified **voltage_values**.

8.56 voltage_range

A **voltage_range** is a range of **voltage_values**. Only the typical value is mandatory.

8.57 voltage_rate

A **voltage_rate** is a change of **voltage_value** within a specific **time_value**.

8.58 voltage_rate_range

A **voltage_rate** is a range of **voltage_rates**. Only the typical value is mandatory.

8.59 voltage_value

A **voltage_value** is a voltage measured in Volts.

8.60 waveform

A **waveform** is a time-variant list of **voltage_ranges** under the specified fixture and DUT conditions.

See keyword [Rising Waveform] and [Falling Waveform].

8.61 waveform_element

A **waveform_element** is the range of **voltage_values** at a specific **time_value**.

See keyword [Rising Waveform] and [Falling Waveform].

9.0 Index

Name	Category	Schema	Line no.
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current_value	TYPE	support_uof	580
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10.0 Attribute Summary

Name	Attribute	Inherited From
ac_terminator_pin_model	AC_capacitance	terminator_pin_model
	AC_resistance	terminator_pin_model
	Vinh	pin_model
	Vinl	pin_model
	Vmeasure	pin_model
	falling_waveforms	pin_model
	ground_clamp	pin_model
	ground_clamp_reference	pin_model
	has_enable	pin_model
	has_polarity	pin_model
	has_ramp	pin_model
	model_name	pin_model
	operating_temperature	pin_model
	power_clamp	pin_model
	power_clamp_reference	pin_model
	pulldown	pin_model
	pulldown_reference	pin_model
	pullup	pin_model
	pullup_reference	pin_model
	reference_capacitance	pin_model
	reference_resistance	pin_model
	resistance_to_ground	terminator_pin_model
	resistance_to_power	terminator_pin_model
	rising_waveforms	pin_model
	signals	pin_model
	silicon_die_capacitance	pin_model
bus	bus_name	-
capacitance_range	maximum_value	-
	minimum_value	-
	typical_value	-
component	component_name	-
	default_capacitance_range	-
	default_inductance_range	-
	default_resistance_range	-
	has_pin_differentials	-
	has_pin_mapping	-
	has_pins	-
	manufacturer_name	-
	uses_package_model	-
current_range	maximum_value	-
	minimum_value	-

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Name	Attribute	Inherited From
	typical_value	-
defined_pin	conforms_to	-
	has_signal	pin
	override_capacitance	pin
	override_inductance	pin
	override_resistance	pin
	pin_name	pin
ground_pin	has_signal	pin
	override_capacitance	pin
	override_inductance	pin
	override_resistance	pin
	pin_name	pin
ibis_file	components	-
	date	-
	disclaimer	-
	file_name	-
	notes	-
	revision	-
	source	-
	status	-
inductance_range	maximum_value	-
	minimum_value	-
	typical_value	-
input_ecl_pin_model	Vinh	pin_model
	Vinl	pin_model
	Vmeasure	pin_model
	falling_waveforms	pin_model
	ground_clamp	pin_model
	ground_clamp_reference	pin_model
	has_enable	pin_model
	has_polarity	pin_model
	has_ramp	pin_model
	model_name	pin_model
	operating_temperature	pin_model
	power_clamp	pin_model
	power_clamp_reference	pin_model
	pulldown	pin_model
	pulldown_reference	pin_model
	pullup	pin_model
	pullup_reference	pin_model
	reference_capacitance	pin_model
	reference_resistance	pin_model

Name	Attribute	Inherited From
	rising_waveforms	pin_model
	signals	pin_model
	silicon_die_capacitance	pin_model
input_output_ecl_pin_model	Vinh	pin_model
	Vinl	pin_model
	Vmeasure	pin_model
	falling_waveforms	pin_model
	ground_clamp	pin_model
	ground_clamp_reference	pin_model
	has_enable	pin_model
	has_polarity	pin_model
	has_ramp	pin_model
	model_name	pin_model
	operating_temperature	pin_model
	power_clamp	pin_model
	power_clamp_reference	pin_model
	pulldown	pin_model
	pulldown_reference	pin_model
	pullup	pin_model
	pullup_reference	pin_model
	reference_capacitance	pin_model
	reference_resistance	pin_model
	rising_waveforms	pin_model
	signals	pin_model
	silicon_die_capacitance	pin_model
input_output_open_drain_pin_model	Vinh	pin_model
	Vinl	pin_model
	Vmeasure	pin_model
	falling_waveforms	pin_model
	ground_clamp	pin_model
	ground_clamp_reference	pin_model
	has_enable	pin_model
	has_polarity	pin_model
	has_ramp	pin_model
	model_name	pin_model
	operating_temperature	pin_model
	power_clamp	pin_model
	power_clamp_reference	pin_model
	pulldown	pin_model
	pulldown_reference	pin_model
	pullup	pin_model
	pullup_reference	pin_model

Name	Attribute	Inherited From
	reference_capacitance	pin_model
	reference_resistance	pin_model
	rising_waveforms	pin_model
	signals	pin_model
	silicon_die_capacitance	pin_model
input_output_open_sink_pin_model	Vinh	pin_model
	Vinl	pin_model
	Vmeasure	pin_model
	falling_waveforms	pin_model
	ground_clamp	pin_model
	ground_clamp_reference	pin_model
	has_enable	pin_model
	has_polarity	pin_model
	has_ramp	pin_model
	model_name	pin_model
	operating_temperature	pin_model
	power_clamp	pin_model
	power_clamp_reference	pin_model
	pulldown	pin_model
	pulldown_reference	pin_model
	pullup	pin_model
	pullup_reference	pin_model
	reference_capacitance	pin_model
	reference_resistance	pin_model
	rising_waveforms	pin_model
	signals	pin_model
	silicon_die_capacitance	pin_model
input_output_open_source_pin_model	Vinh	pin_model
	Vinl	pin_model
	Vmeasure	pin_model
	falling_waveforms	pin_model
	ground_clamp	pin_model
	ground_clamp_reference	pin_model
	has_enable	pin_model
	has_polarity	pin_model
	has_ramp	pin_model
	model_name	pin_model
	operating_temperature	pin_model
	power_clamp	pin_model
	power_clamp_reference	pin_model
	pulldown	pin_model
	pulldown_reference	pin_model

Name	Attribute	Inherited From
	pullup	pin_model
	pullup_reference	pin_model
	reference_capacitance	pin_model
	reference_resistance	pin_model
	rising_waveforms	pin_model
	signals	pin_model
	silicon_die_capacitance	pin_model
input_output_pin_model	Vinh	pin_model
	Vinl	pin_model
	Vmeasure	pin_model
	falling_waveforms	pin_model
	ground_clamp	pin_model
	ground_clamp_reference	pin_model
	has_enable	pin_model
	has_polarity	pin_model
	has_ramp	pin_model
	model_name	pin_model
	operating_temperature	pin_model
	power_clamp	pin_model
	power_clamp_reference	pin_model
	pulldown	pin_model
	pulldown_reference	pin_model
	pullup	pin_model
	pullup_reference	pin_model
	reference_capacitance	pin_model
	reference_resistance	pin_model
	rising_waveforms	pin_model
	signals	pin_model
	silicon_die_capacitance	pin_model
input_pin_model	Vinh	pin_model
	Vinl	pin_model
	Vmeasure	pin_model
	falling_waveforms	pin_model
	ground_clamp	pin_model
	ground_clamp_reference	pin_model
	has_enable	pin_model
	has_polarity	pin_model
	has_ramp	pin_model
	model_name	pin_model
	operating_temperature	pin_model
	power_clamp	pin_model
	power_clamp_reference	pin_model

Name	Attribute	Inherited From
	pulldown	pin_model
	pulldown_reference	pin_model
	pullup	pin_model
	pullup_reference	pin_model
	reference_capacitance	pin_model
	reference_resistance	pin_model
	rising_waveforms	pin_model
	signals	pin_model
	silicon_die_capacitance	pin_model
not_connected_pin	has_signal	pin
	override_capacitance	pin
	override_inductance	pin
	override_resistance	pin
	pin_name	pin
open_drain_pin_model	Vinh	pin_model
	Vinl	pin_model
	Vmeasure	pin_model
	falling_waveforms	pin_model
	ground_clamp	pin_model
	ground_clamp_reference	pin_model
	has_enable	pin_model
	has_polarity	pin_model
	has_ramp	pin_model
	model_name	pin_model
	operating_temperature	pin_model
	power_clamp	pin_model
	power_clamp_reference	pin_model
	pulldown	pin_model
	pulldown_reference	pin_model
	pullup	pin_model
	pullup_reference	pin_model
	reference_capacitance	pin_model
	reference_resistance	pin_model
	rising_waveforms	pin_model
	signals	pin_model
	silicon_die_capacitance	pin_model
open_sink_pin_model	Vinh	pin_model
	Vinl	pin_model
	Vmeasure	pin_model
	falling_waveforms	pin_model
	ground_clamp	pin_model
	ground_clamp_reference	pin_model

Name	Attribute	Inherited From
	has_enable	pin_model
	has_polarity	pin_model
	has_ramp	pin_model
	model_name	pin_model
	operating_temperature	pin_model
	power_clamp	pin_model
	power_clamp_reference	pin_model
	pulldown	pin_model
	pulldown_reference	pin_model
	pullup	pin_model
	pullup_reference	pin_model
	reference_capacitance	pin_model
	reference_resistance	pin_model
	rising_waveforms	pin_model
	signals	pin_model
	silicon_die_capacitance	pin_model
open_source_pin_model	Vinh	pin_model
	Vinl	pin_model
	Vmeasure	pin_model
	falling_waveforms	pin_model
	ground_clamp	pin_model
	ground_clamp_reference	pin_model
	has_enable	pin_model
	has_polarity	pin_model
	has_ramp	pin_model
	model_name	pin_model
	operating_temperature	pin_model
	power_clamp	pin_model
	power_clamp_reference	pin_model
	pulldown	pin_model
	pulldown_reference	pin_model
	pullup	pin_model
	pullup_reference	pin_model
	reference_capacitance	pin_model
	reference_resistance	pin_model
	rising_waveforms	pin_model
	signals	pin_model
	silicon_die_capacitance	pin_model
output_ecl_pin_model	Vinh	pin_model
	Vinl	pin_model
	Vmeasure	pin_model
	falling_waveforms	pin_model

Name	Attribute	Inherited From
	ground_clamp	pin_model
	ground_clamp_reference	pin_model
	has_enable	pin_model
	has_polarity	pin_model
	has_ramp	pin_model
	model_name	pin_model
	operating_temperature	pin_model
	power_clamp	pin_model
	power_clamp_reference	pin_model
	pulldown	pin_model
	pulldown_reference	pin_model
	pullup	pin_model
	pullup_reference	pin_model
	reference_capacitance	pin_model
	reference_resistance	pin_model
	rising_waveforms	pin_model
	signals	pin_model
	silicon_die_capacitance	pin_model
output_pin_model	Vinh	pin_model
	Vinl	pin_model
	Vmeasure	pin_model
	falling_waveforms	pin_model
	ground_clamp	pin_model
	ground_clamp_reference	pin_model
	has_enable	pin_model
	has_polarity	pin_model
	has_ramp	pin_model
	model_name	pin_model
	operating_temperature	pin_model
	power_clamp	pin_model
	power_clamp_reference	pin_model
	pulldown	pin_model
	pulldown_reference	pin_model
	pullup	pin_model
	pullup_reference	pin_model
	reference_capacitance	pin_model
	reference_resistance	pin_model
	rising_waveforms	pin_model
	signals	pin_model
	silicon_die_capacitance	pin_model
package_model	capacitance_matrix	-
	description	-

Name	Attribute	Inherited From
	inductance_matrix	-
	model_name	-
	number_of_pins	-
	package_manufacturer_name	-
	package_pins	-
	part_manufacturer_name	-
	resistance_matrix	-
package_pin	pin_name	-
pin	has_signal	-
	override_capacitance	-
	override_inductance	-
	override_resistance	-
	pin_name	-
pin_differential	delay	-
	inverting_pin	-
	non_inverting_pin	-
	voltage_differential	-
pin_map	for_pin	-
	ground_clamp	-
	power_clamp	-
	pulldown_reference	-
	pullup_reference	-
pin_mapping	members	-
pin_model	Vinh	-
	Vinl	-
	Vmeasure	-
	falling_waveforms	-
	ground_clamp	-
	ground_clamp_reference	-
	has_enable	-
	has_polarity	-
	has_ramp	-
	model_name	-
	operating_temperature	-
	power_clamp	-
	power_clamp_reference	-
	pulldown	-
	pulldown_reference	-
	pullup	-
	pullup_reference	-
	reference_capacitance	-
	reference_resistance	-

Name	Attribute	Inherited From
	rising_waveforms	-
	signals	-
	silicon_die_capacitance	-
pin_to_pin_capacitance	between_pins	-
	has_capacitance	-
pin_to_pin_inductance	between_pins	-
	has_inductance	-
pin_to_pin_resistance	between_pins	-
	has_resistance	-
power_pin	has_signal	pin
	override_capacitance	pin
	override_inductance	pin
	override_resistance	pin
	pin_name	pin
predefined_pin	has_signal	pin
	override_capacitance	pin
	override_inductance	pin
	override_resistance	pin
	pin_name	pin
ramp	fall_ramp	-
	load_resistance	-
	rise_ramp	-
resistance_range	maximum_value	-
	minimum_value	-
	typical_value	-
signal	signal_name	-
temperature_range	maximum_value	-
	minimum_value	-
	typical_value	-
terminator_pin_model	AC_capacitance	-
	AC_resistance	-
	Vinh	pin_model
	Vinl	pin_model
	Vmeasure	pin_model
	falling_waveforms	pin_model
	ground_clamp	pin_model
	ground_clamp_reference	pin_model
	has_enable	pin_model
	has_polarity	pin_model
	has_ramp	pin_model
	model_name	pin_model
	operating_temperature	pin_model

Name	Attribute	Inherited From
	power_clamp	pin_model
	power_clamp_reference	pin_model
	pulldown	pin_model
	pulldown_reference	pin_model
	pullup	pin_model
	pullup_reference	pin_model
	reference_capacitance	pin_model
	reference_resistance	pin_model
	resistance_to_ground	-
	resistance_to_power	-
	rising_waveforms	pin_model
	signals	pin_model
	silicon_die_capacitance	pin_model
time_range	maximum_value	-
	minimum_value	-
	typical_value	-
tri_state_pin_model	Vinh	pin_model
	Vinl	pin_model
	Vmeasure	pin_model
	falling_waveforms	pin_model
	ground_clamp	pin_model
	ground_clamp_reference	pin_model
	has_enable	pin_model
	has_polarity	pin_model
	has_ramp	pin_model
	model_name	pin_model
	operating_temperature	pin_model
	power_clamp	pin_model
	power_clamp_reference	pin_model
	pulldown	pin_model
	pulldown_reference	pin_model
	pullup	pin_model
	pullup_reference	pin_model
	reference_capacitance	pin_model
	reference_resistance	pin_model
	rising_waveforms	pin_model
	signals	pin_model
	silicon_die_capacitance	pin_model
voltage_current_map	current	-
	for_voltage	-
voltage_current_table	members	-
voltage_range	maximum_value	-

Name	Attribute	Inherited From
	minimum_value	-
	typical_value	-
voltage_rate	in_time	-
	voltage_change	-
voltage_rate_range	maximum_value	-
	minimum_value	-
	typical_value	-
waveform	dut_capacitance	-
	dut_inductance	-
	dut_resistance	-
	fixture_capacitance	-
	fixture_inductance	-
	fixture_resistance	-
	fixture_voltage	-
	members	-
waveform_element	at_time	-
	voltage	-

11.0 Relationship Summary

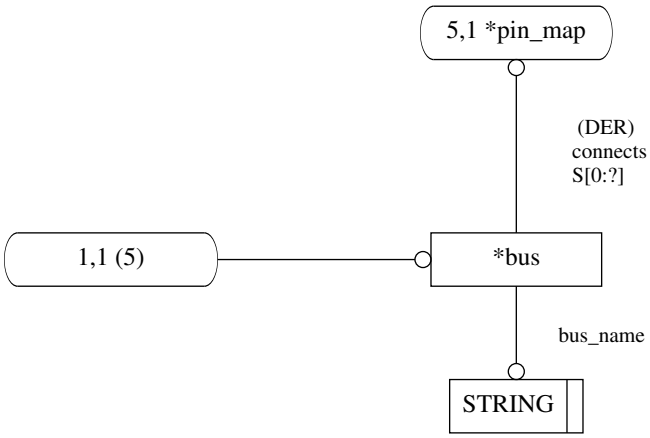
entity/type	directly referenced by	no. of times
ac_terminator_pin_model	-	-
bus	pin_map	4
capacitance_range	ac_terminator_pin_model	1
	component	1
	pin_model	1
	terminator_pin_model	1
capacitance_value	capacitance_range	3
	pin	1
	pin_model	1
	pin_to_pin_capacitance	1
	waveform	2
component	ibis_file	1
current_range	voltage_current_map	1
current_value	current_range	3
defined_pin	-	-
enable	pin_model	1
file_status	ibis_file	1
ground_pin	-	-
ibis_file	-	-
inductance_range	component	1
inductance_value	inductance_range	3
	pin	1
	pin_to_pin_inductance	1
	waveform	2
input_ecl_pin_model	-	-
input_output_ecl_pin_model	-	-
input_output_open_drain_pin_model	-	-
input_output_open_sink_pin_model	-	-
input_output_open_source_pin_model	-	-
input_output_pin_model	-	-
input_pin_model	-	-
non_negative_real	capacitance_value	1
	inductance_value	1
	resistance_value	1
	time_value	1
not_connected_pin	-	-
open_drain_pin_model	-	-
open_sink_pin_model	-	-
open_source_pin_model	-	-
output_ecl_pin_model	-	-
output_pin_model	-	-

entity/type	directly referenced by	no. of times
package_model	component	1
package_pin	package_model	1
	pin_to_pin_capacitance	1
	pin_to_pin_inductance	1
	pin_to_pin_resistance	1
pin	component	1
	pin_differential	2
	pin_map	1
pin_differential	component	1
pin_map	bus	1
	pin_mapping	1
pin_mapping	component	1
pin_model	defined_pin	1
pin_to_pin_capacitance	package_model	1
pin_to_pin_inductance	package_model	1
pin_to_pin_resistance	package_model	1
polarity	pin_model	1
positive_integer_value	package_model	2
power_pin	-	-
predefined_pin	-	-
ramp	input_output_ecl_pin_model	1
	input_output_open_drain_pin_model	1
	input_output_open_sink_pin_model	1
	input_output_open_source_pin_model	1
	input_output_pin_model	1
	open_drain_pin_model	1
	open_sink_pin_model	1
	open_source_pin_model	1
	output_ecl_pin_model	1
	output_pin_model	1
	pin_model	1
	tri_state_pin_model	1
resistance_range	ac_terminator_pin_model	1
	component	1
	terminator_pin_model	3
resistance_value	pin	1
	pin_model	1
	pin_to_pin_resistance	1
	ramp	1
	resistance_range	3
	waveform	3
signal	pin	1

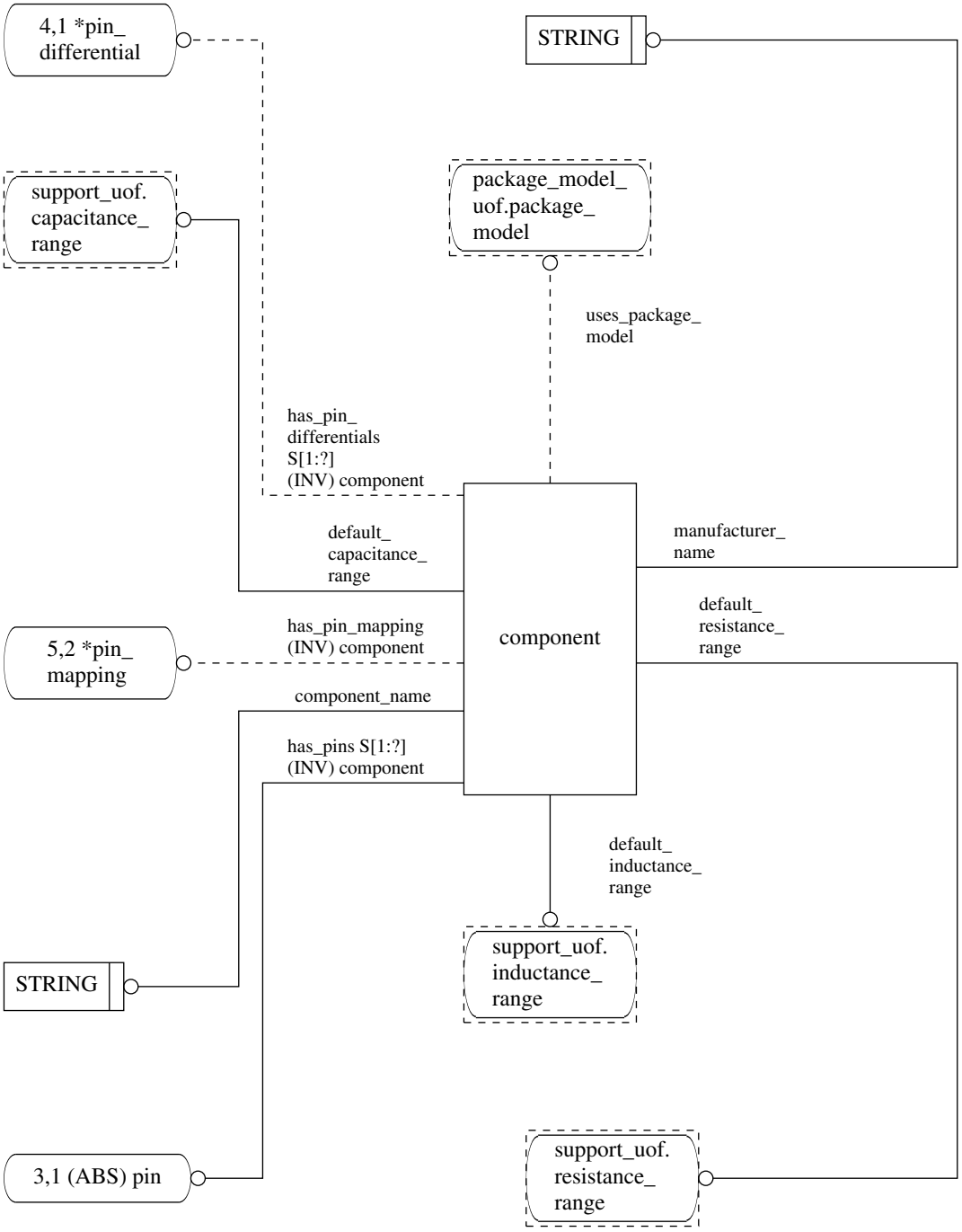
entity/type	directly referenced by	no. of times
	pin_model	1
temperature_range	pin_model	1
temperature_value	temperature_range	3
terminator_pin_model	-	-
time_range	pin_differential	1
time_value	time_range	3
	voltage_rate	1
	waveform_element	1
tri_state_pin_model	-	-
voltage_current_map	voltage_current_table	1
voltage_current_table	pin_model	4
voltage_range	pin_model	4
	waveform_element	1
voltage_rate	voltage_rate_range	3
voltage_rate_range	ramp	2
voltage_value	input_ecl_pin_model	2
	input_output_ecl_pin_model	2
	input_output_open_drain_pin_model	2
	input_output_open_sink_pin_model	2
	input_output_open_source_pin_model	2
	input_output_pin_model	2
	input_pin_model	2
	pin_differential	1
	pin_model	3
	voltage_current_map	1
	voltage_range	3
	voltage_rate	1
waveform	pin_model	2
waveform_element	waveform	1

12.0 EXPRESS-G for Component UoF

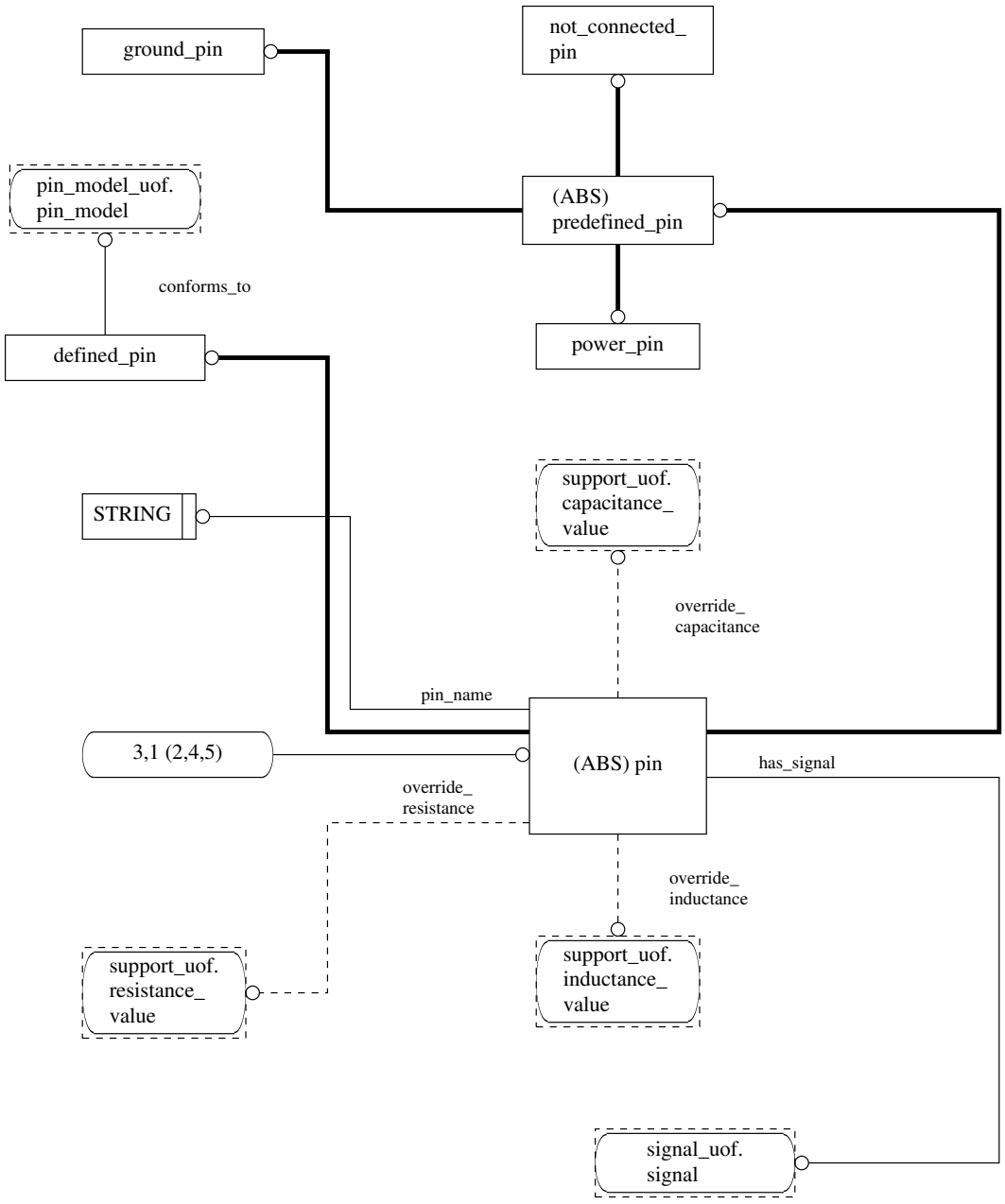
12.1 Bus



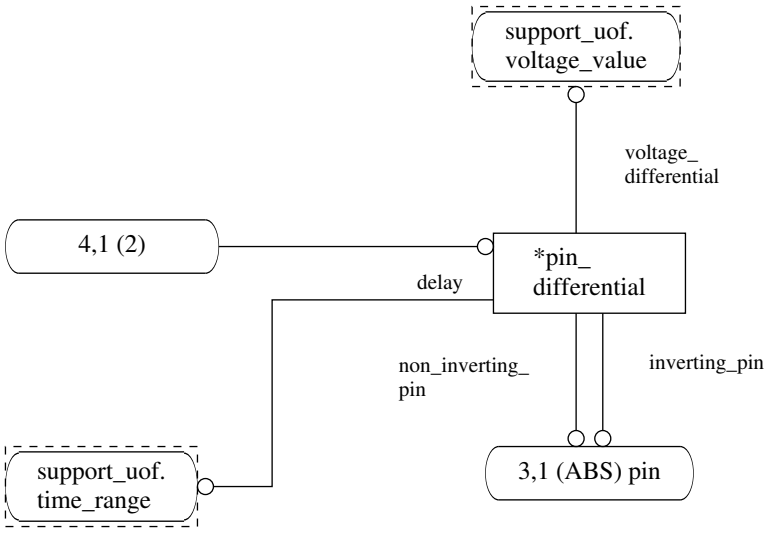
12.2 Component



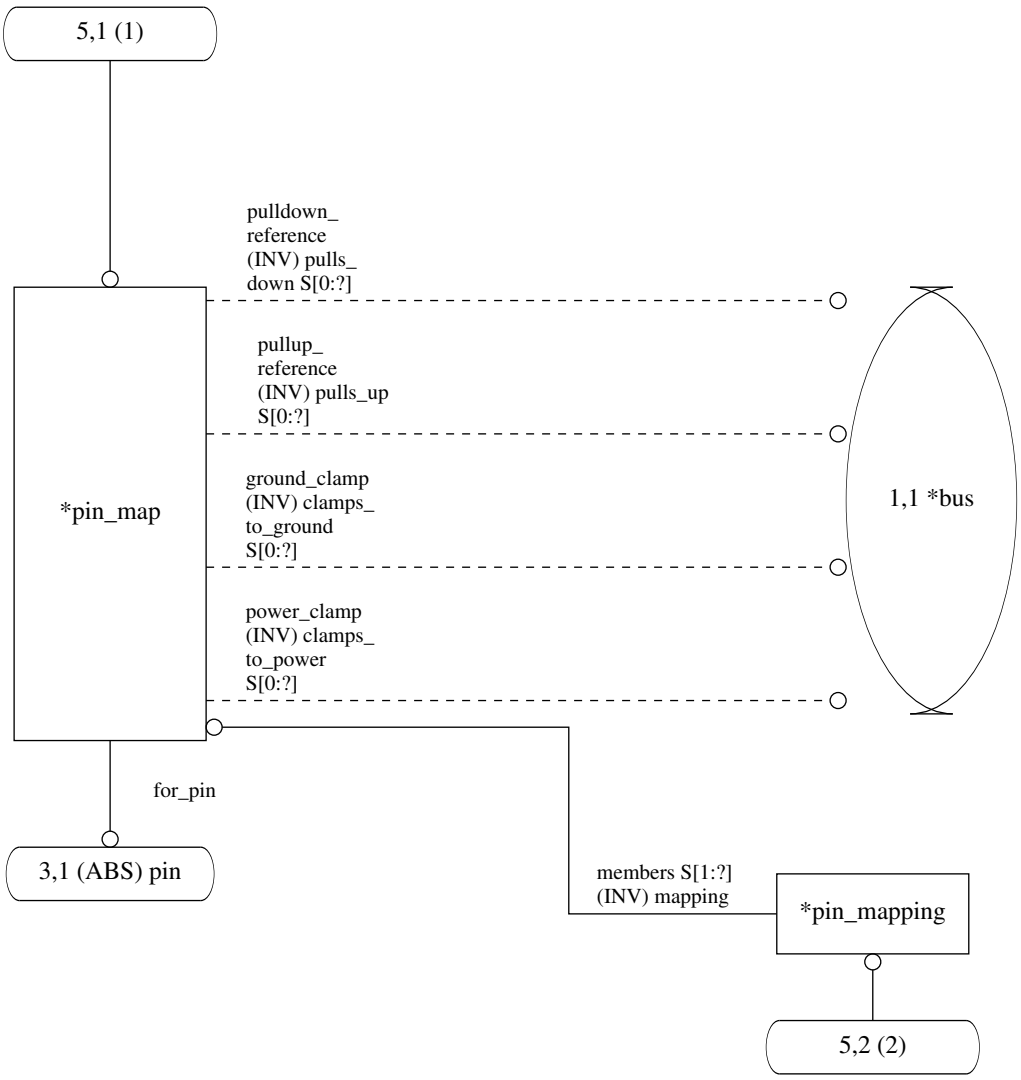
12.3 Pin


ground_pin
not_connected_
pin
pin_model_uof.
pin_model
(ABS)
predefined_pin
conforms_to
power_pin
defined_pin
STRING
support_uof.
capacitance_
value
override_
capacitance
pin_name
3,1 (2,4,5)
(ABS) pin
has_signal
override_
resistance
override_
inductance
support_uof.
resistance_
value
support_uof.
inductance_
value
signal_uof.
signal

12.4 Pin Differential



12.5 Pin Map



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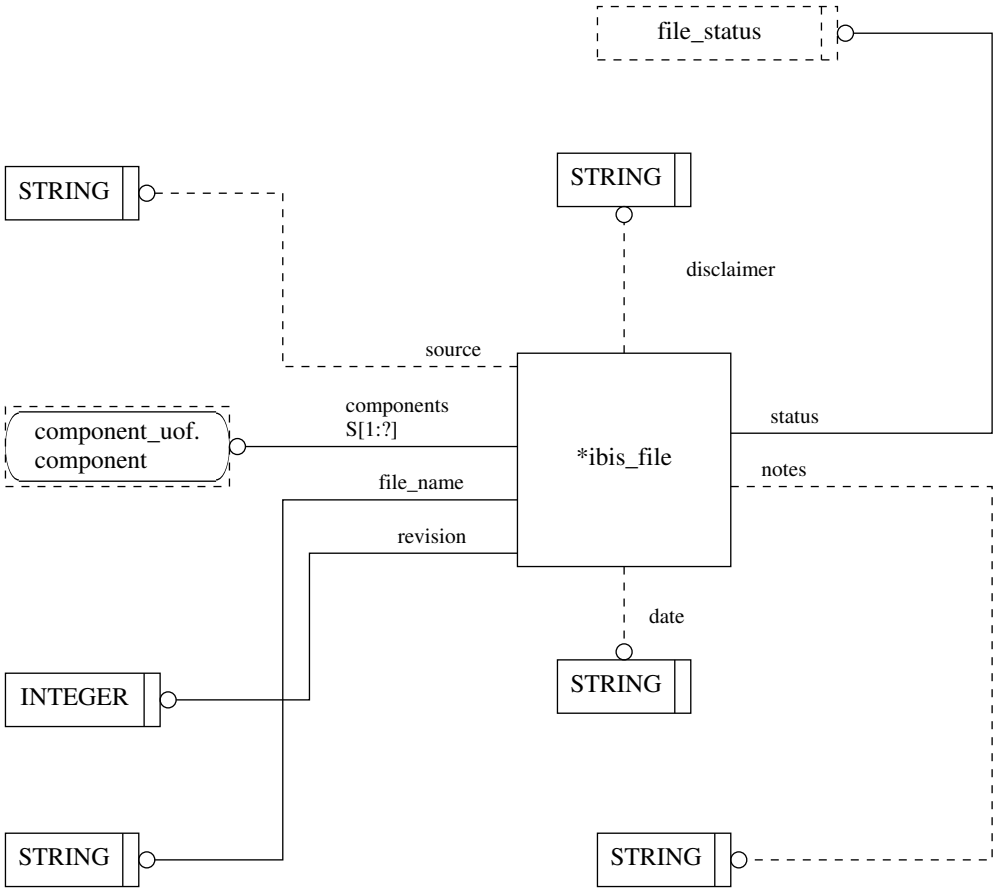
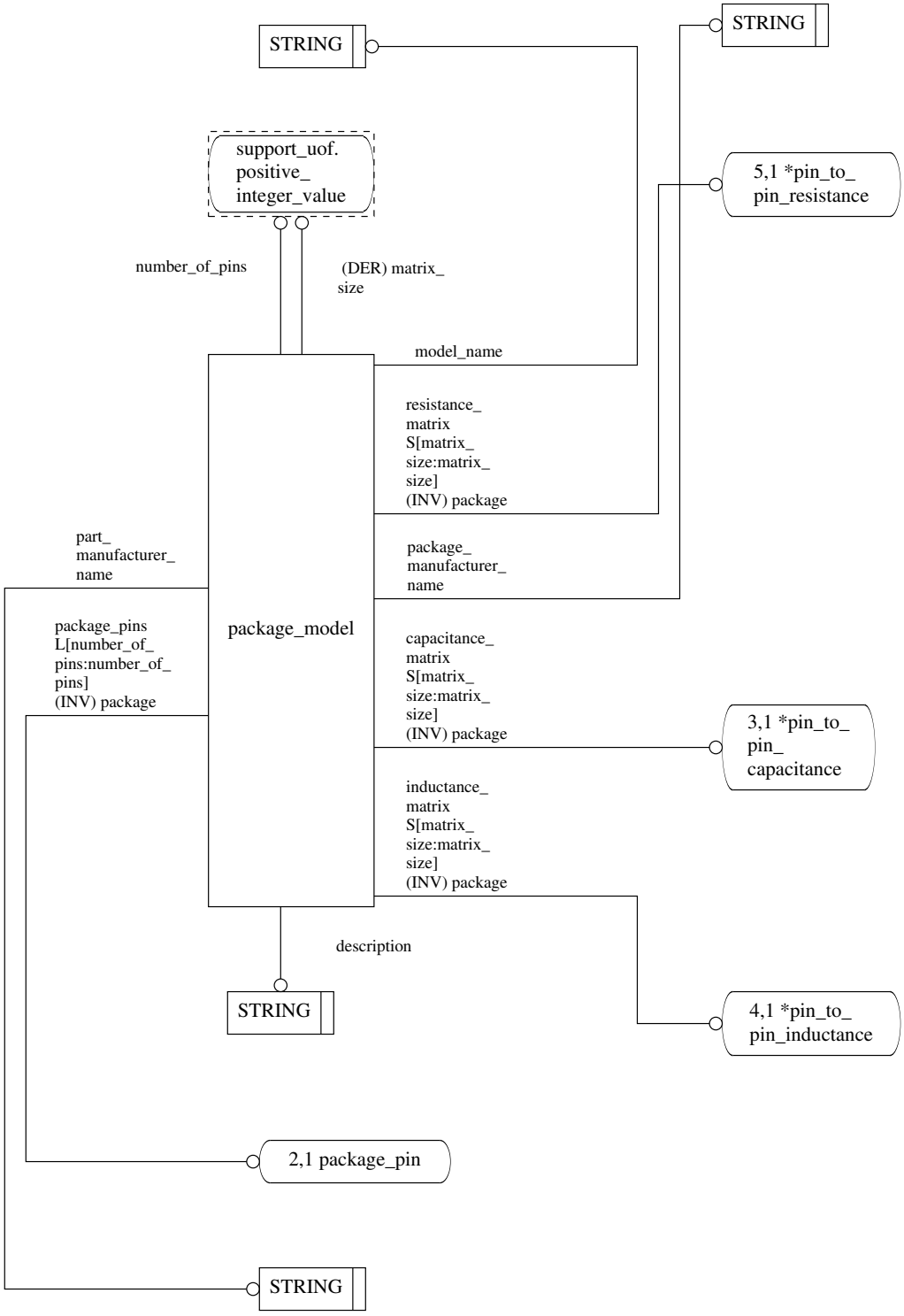
13.0 EXPRESS-G for File UoF

13.1 IBIS File

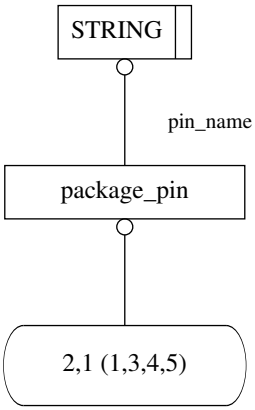


14.0 EXPRESS-G for Package Model UoF

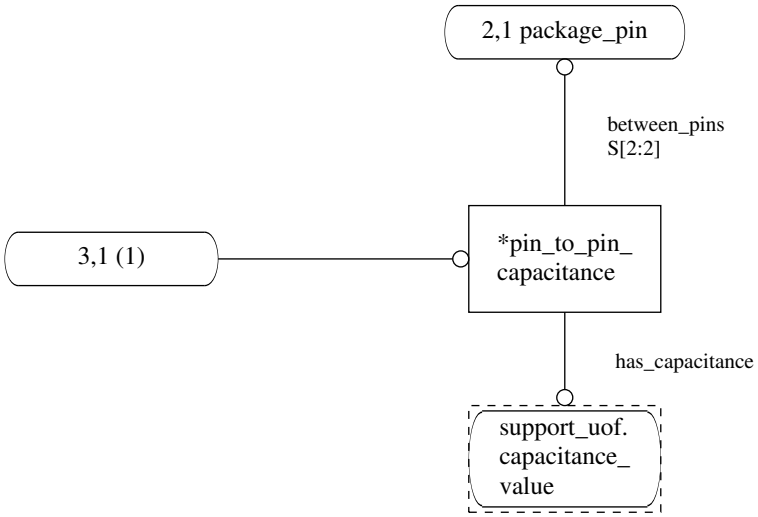
14.1 Package Model



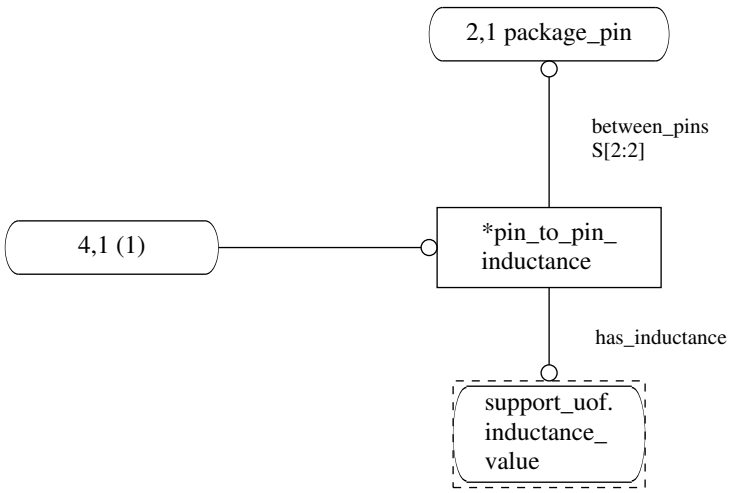
14.2 Package Pin



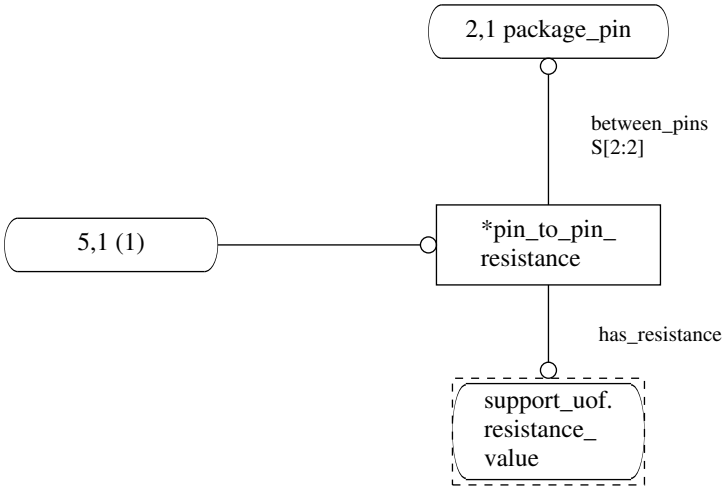
14.3 Pin to Pin Capacitance



14.4 Pin to Pin Inductance

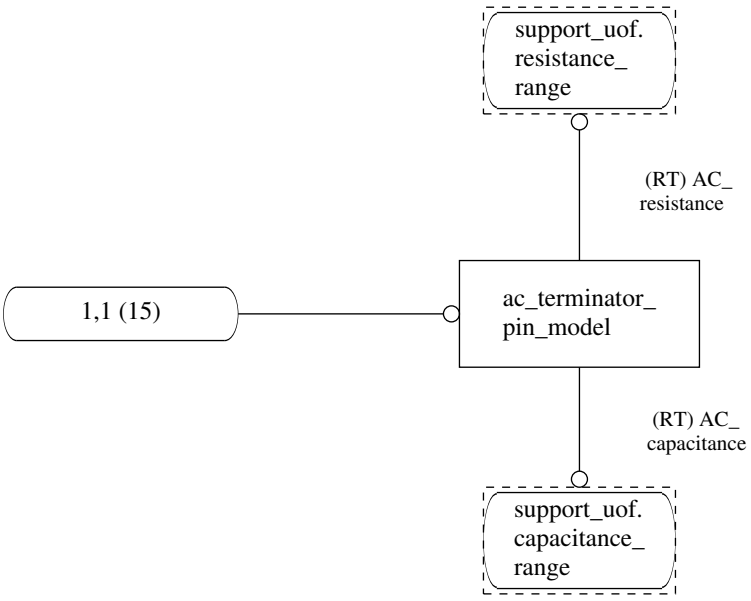


14.5 Pin to Pin Resistance

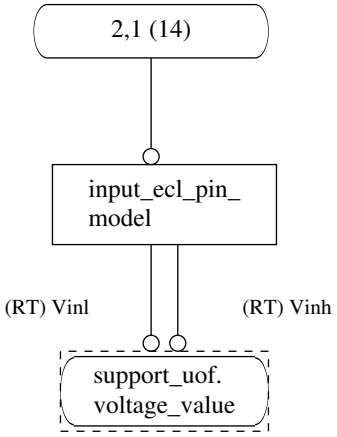


15.0 EXPRESS-G for Pin Model UoF

15.1 AC Terminator Pin Model



15.2 Input ECL Pin Model



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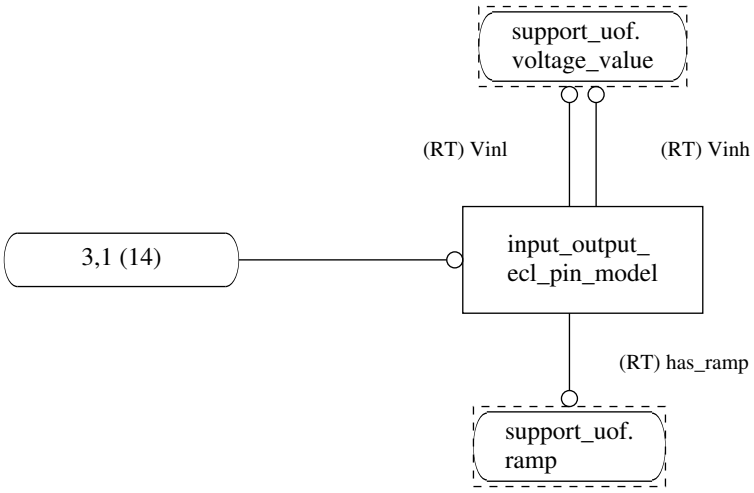
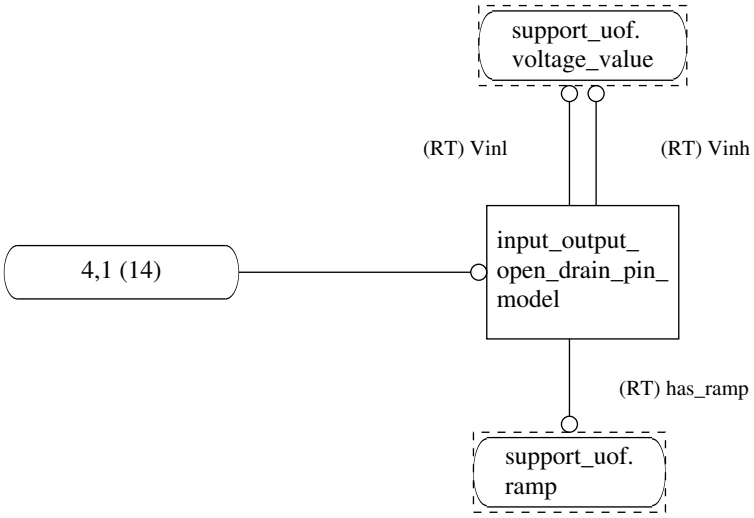
15.3 Input/Output ECL Pin Model



15.4 Input/Output Open Drain Pin Model



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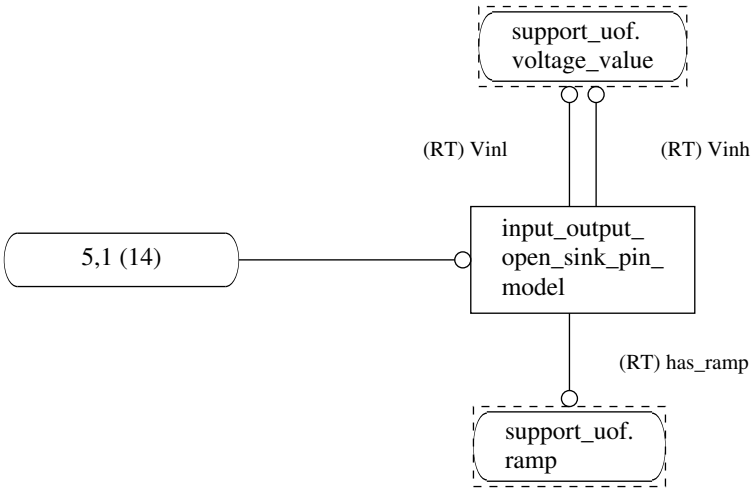
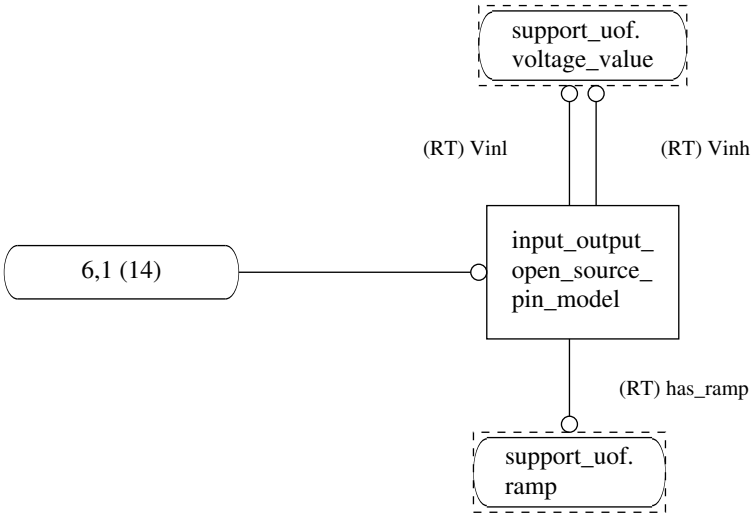
15.5 Input/Output Open Sink Pin Model



15.6 Input/Output Open Source Pin Model



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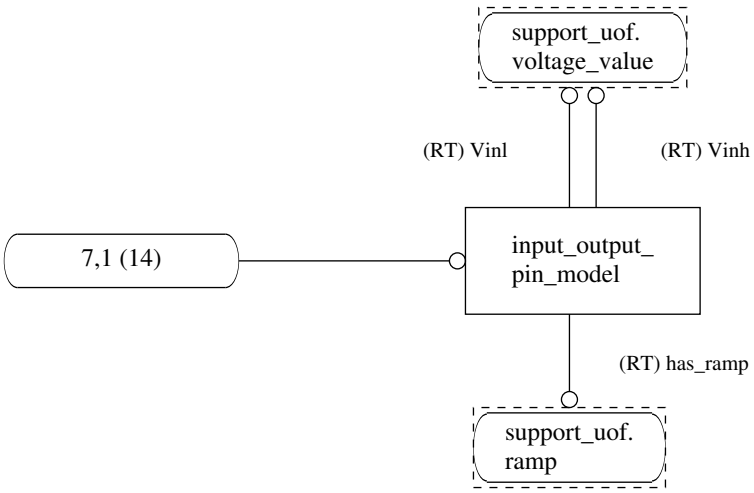
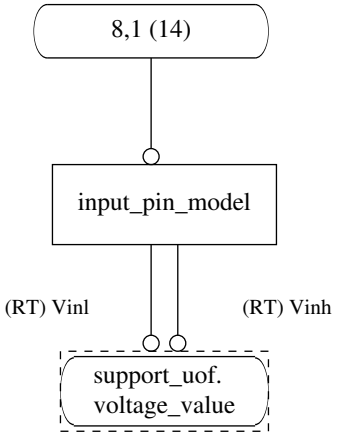
15.7 Input/Output Pin Model



15.8 Input Pin Model



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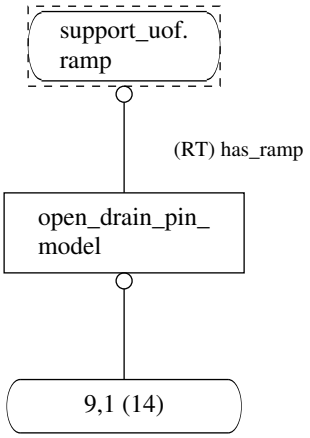
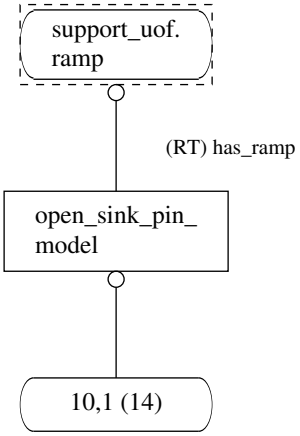
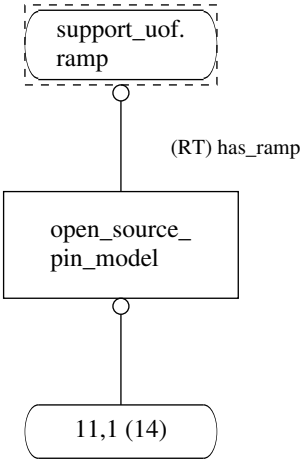
15.9 Open Drain Pin Model



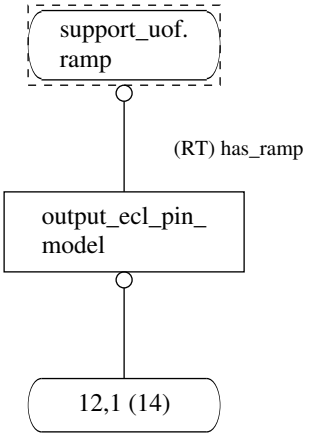
15.10 Open Sink Pin Model



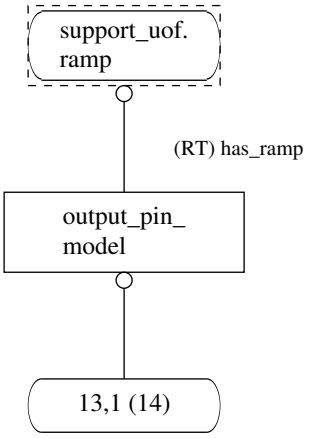
15.11 Open Source Pin Model



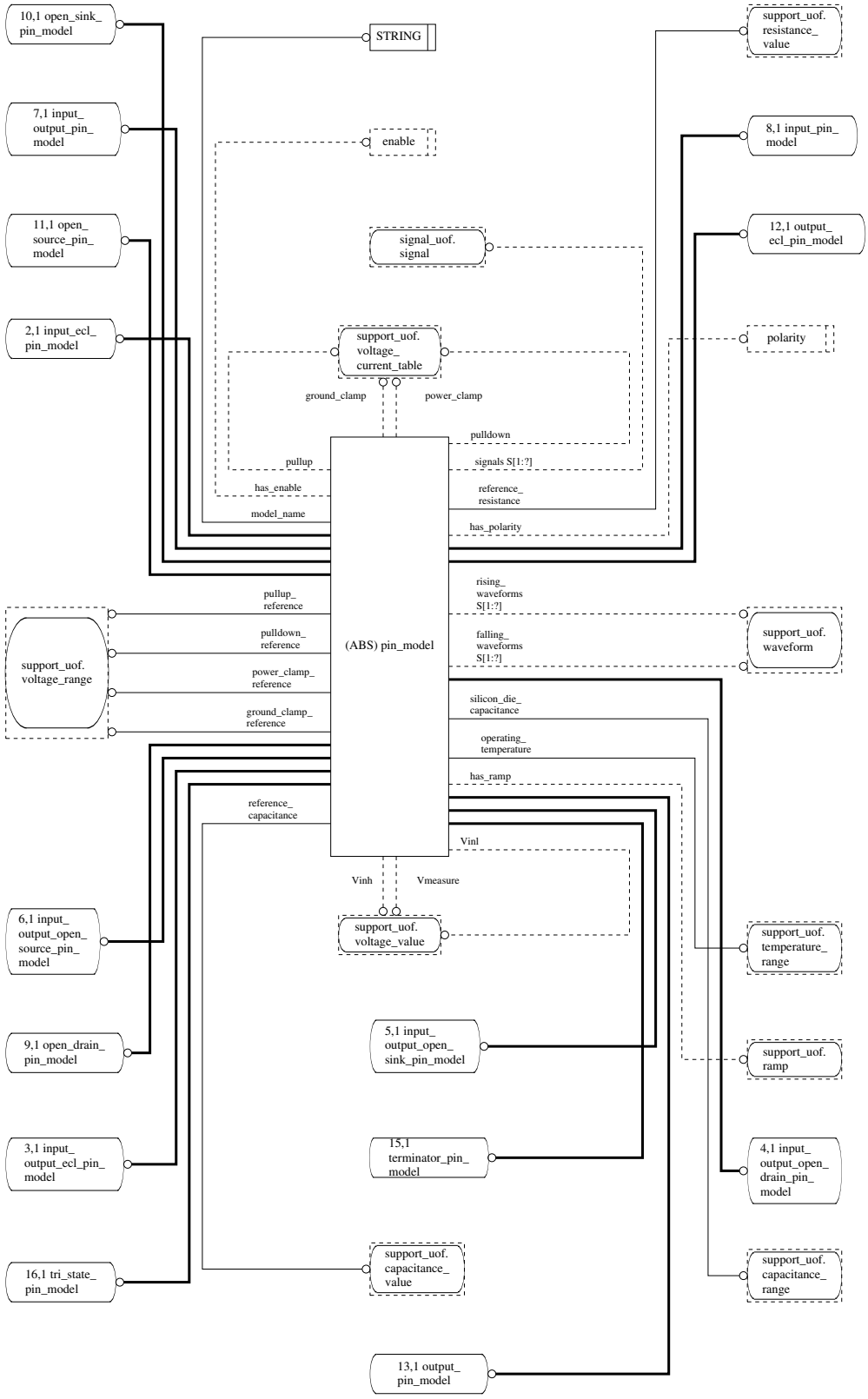
15.12 Output ECL Pin Model



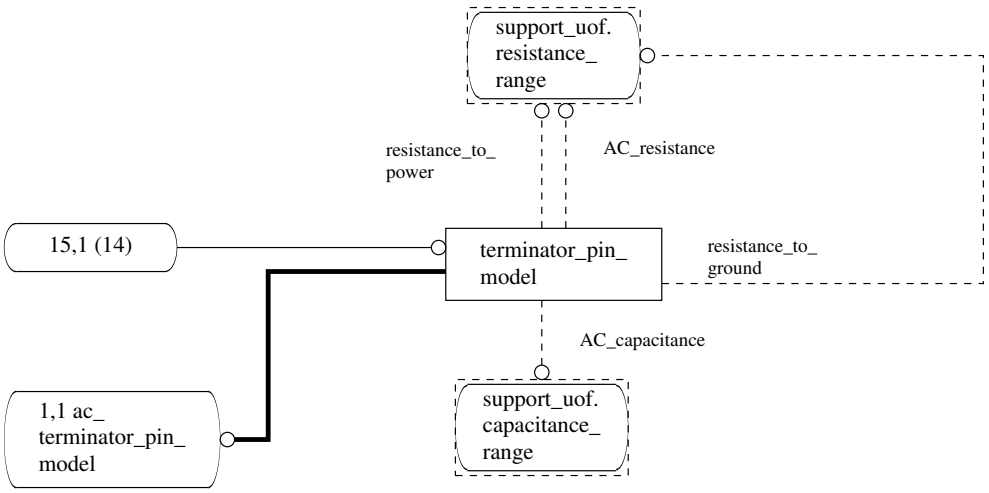
15.13 Output Pin Model



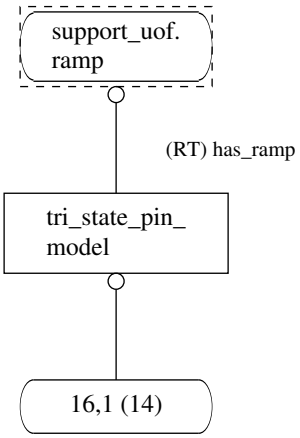
15.14 Pin Model



15.15 Terminator Pin Model



15.16 Tri-State Pin Model



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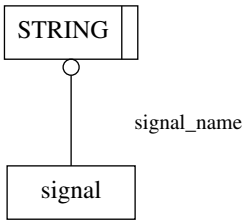
16.0 EXPRESS-G for Signal UoF

16.1 Signal



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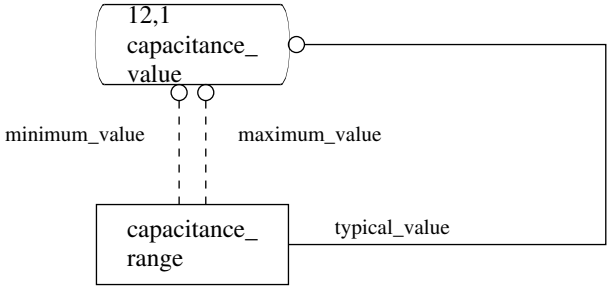
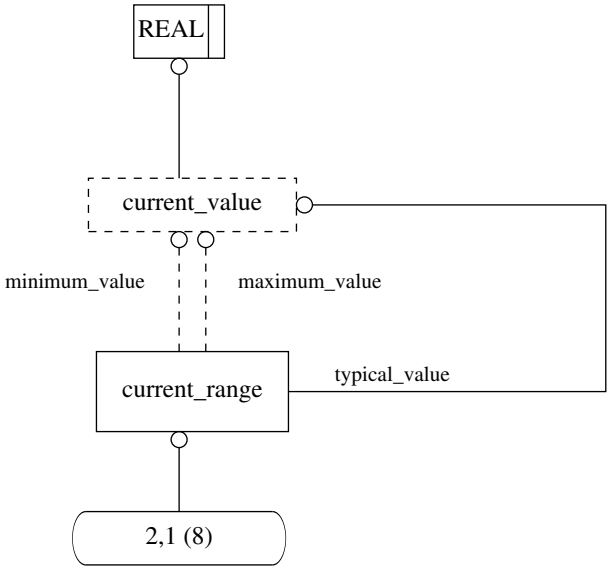
17.0 EXPRESS-G for Support UoF

17.1 Capacitance Range



17.2 Current Range



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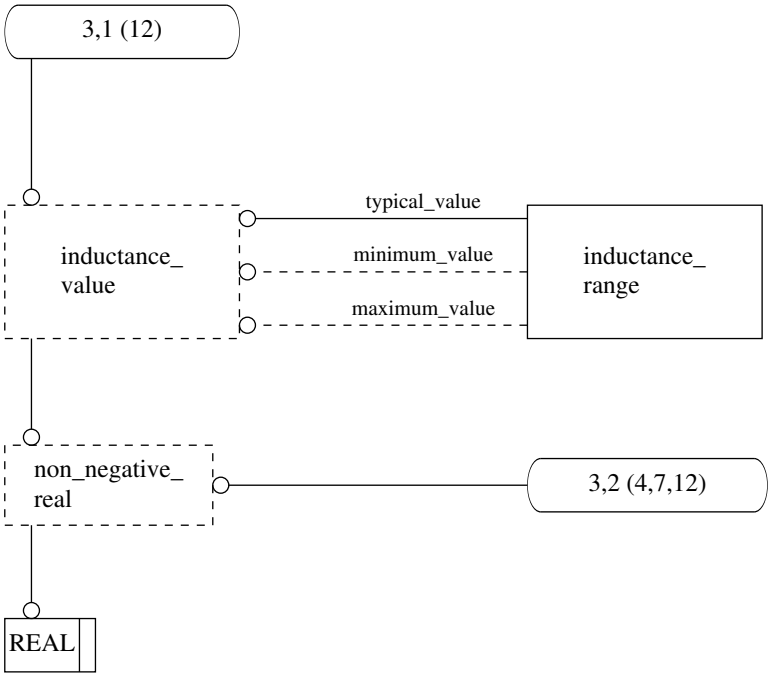
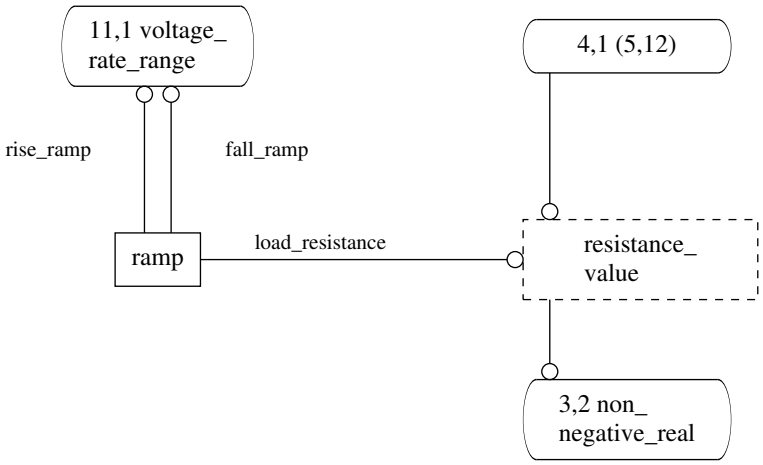
17.3 Inductance Range



17.4 Ramp



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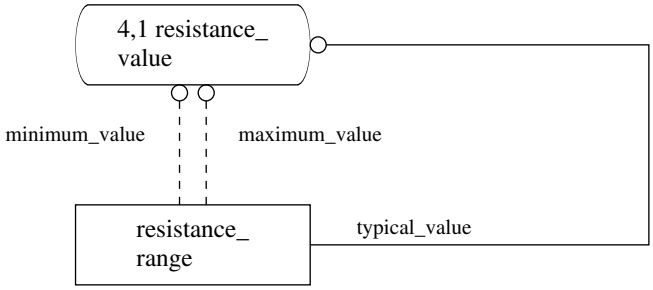
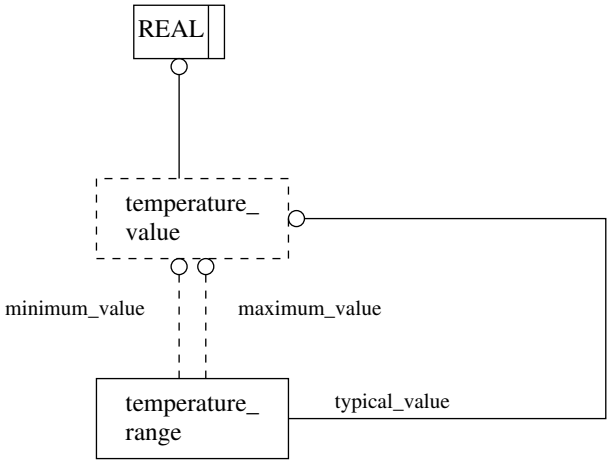
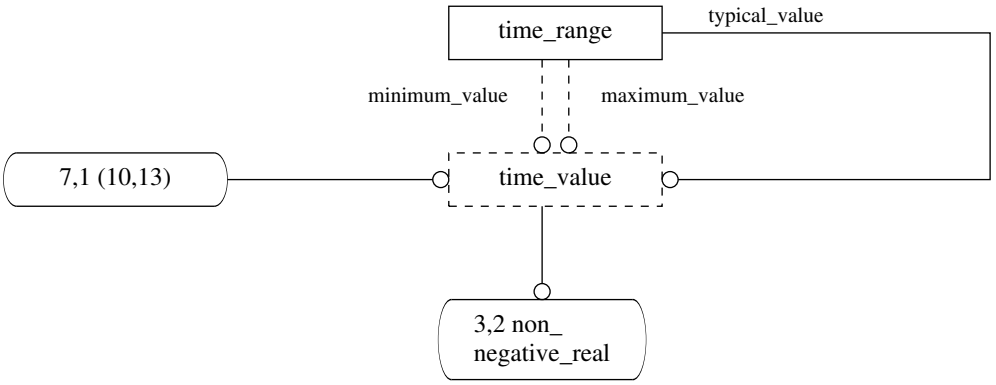
17.5 Resistance Range



17.6 Temperature Range



17.7 Time Range



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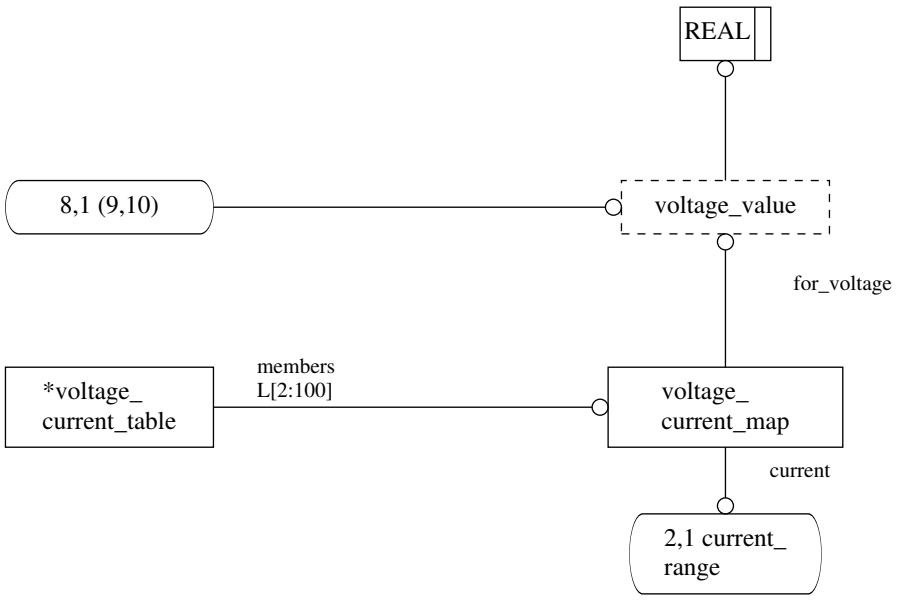
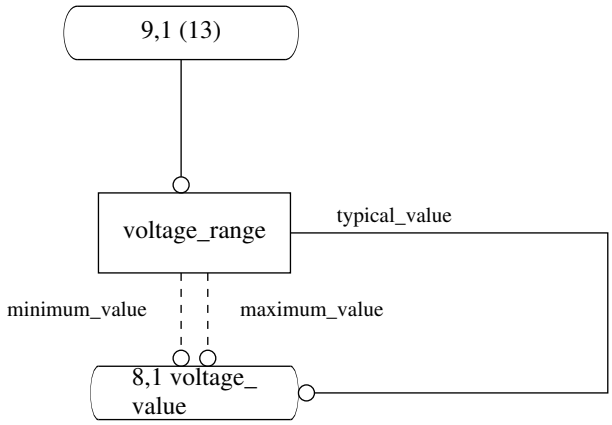
17.8 Voltage Current Table



17.9 Voltage Range



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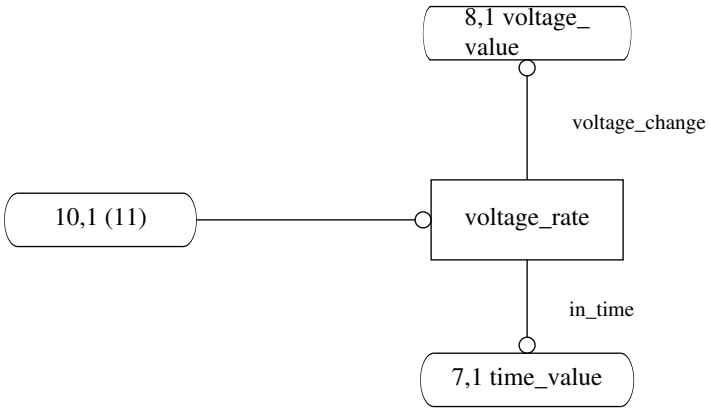
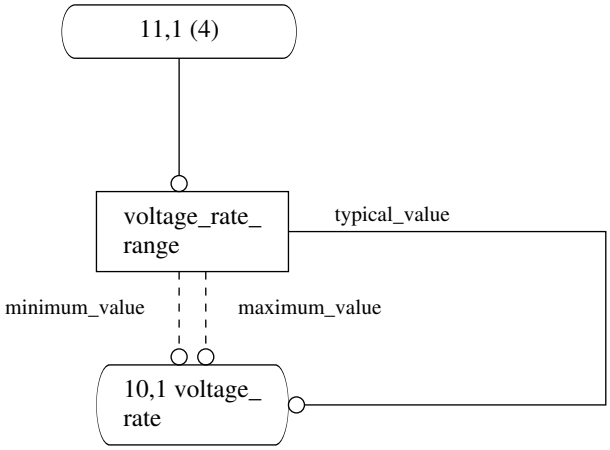
17.10 Voltage Rate



17.11 Voltage Rate Range



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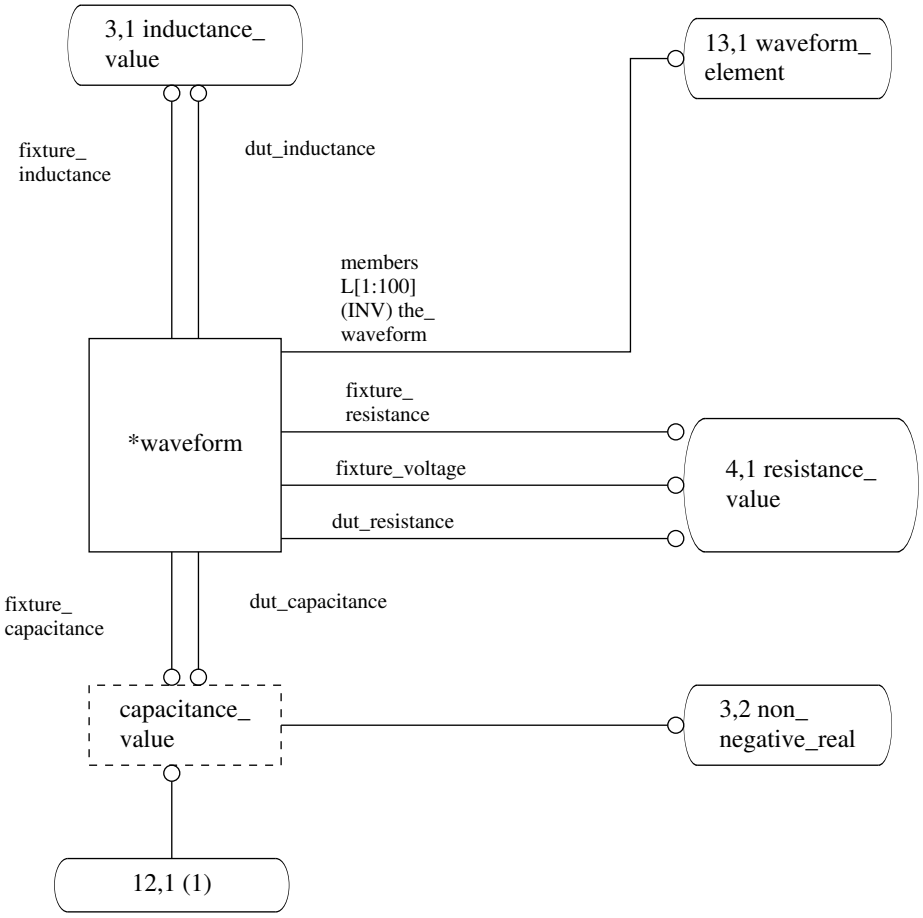
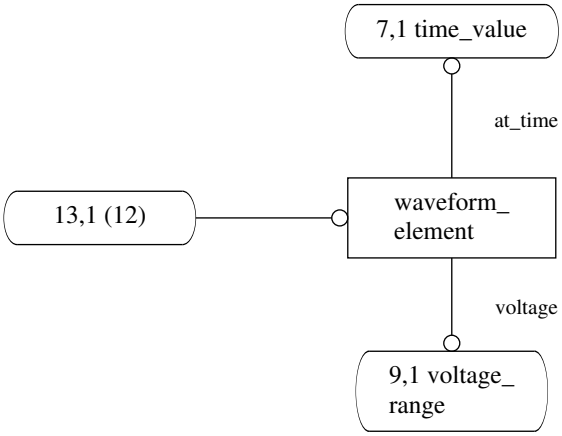
17.12 Waveform



17.13 Waveform Element